ODIN Q_FE registers (Base address 0x4000)

Version: 2.3 2006.07.10

Address	Bits	Register	Read/Write	Explanation	Remark	Default
000		Not used				0
004	0	RST_MAC		Reset GBE MAC		0
008	0	R_FE_ENB		Enable ODIN Front-End		0
	1	R_SINGLE_DEST_ENB		Enable use of single MEP destination	(Move to Q_L1)	0
00C	1 .. 0	P_GBE_PORT_0		GbE port for FE channel 0		0
	3 .. 2	P_GBE_PORT_1		GbE port for FE channel 1		0
010	23 .. 0	P_MAC_SRC_OUI_0		MAC source OUI for FE channel 0		0
014	23 .. 0	P_MAC_SRC_DID_0		MAC source DID for FE channel 0		0
018	23 .. 0	P_MAC_SRC_OUI_1		MAC source OUI for FE channel 1		0
01C	23 .. 0	P_MAC_SRC_DID_1		MAC source DID for FE channel 1		0
020	23 .. 0	P_MAC_DEST_OUI_0		MAC destination OUI for FE channel 0		0
024	23 .. 0	P_MAC_DEST_DID_0		MAC destination DID for FE channel 0		0
028	23 .. 0	P_MAC_DEST_OUI_1		MAC destination OUI for FE channel 1		0
02C	23 .. 0	P_MAC_DEST_DID_1		MAC destination DID for FE channel 1		0
030	15 .. 0	P_ETH_TYPE		Ethernet type		0
034	3 .. 0	P_IP_HDR_LEN		IP header length		0
	7 .. 4	P_IP_VERSION		IP version		0
	15 .. 8	P_IP_SERVICE		Type of service		0
	23 .. 16	P_IP_TTL		IP time to live		0
	31 .. 24	P_IP_PROTOCOL		IP protocol		0
038	31 .. 0	P_IP_SRCADDR_0		IP source address for FE channel 0		0
03C	31 .. 0	P_IP_SRCADDR_1		IP source address for FE channel 1		0
040	31 .. 0	P_IP_DESTADDR_0		IP destination address for FE channel 0		0
044	31 .. 0	P_IP_DESTADDR_1		IP destination address for FE channel 1		0
048	15 .. 0	P_BANK_SRCID		Bank source ID	ODIN serial number	0
04C	31 .. 0	R_PARTITION_ID		Partition identifier for the run		0
050	31 .. 0	R_RUN_NUMBER		Run number		0
054	31 .. 0	R_EVENT_TYPE		Event type = run type		0
058	23 .. 0	R_GPS_TIME_H		Upper 24 bits of the 64 bits UTC time		0
05C		Not used				
060	31 .. 0	RST_SEL_CNT		Reset selected counters	One bit per counter	0
0A0	10 .. 0	INT_MACCNF_ADDR		MAC configuration register address		0

0A4	31 .. 0	INT_MACCNF_DATA		MAC configuration data to register written in 0x40A0		0
0A8	0	S_FEB_EMPTY	RO	FEB empty status		
	1	S_MB_EMPTY	RO	MEP buffer empty status		
	2	S_GBE_EMPTY	RO	GbE transmission buffer empty		
	3	S_GBE_FULL	RO	GbE transmission buffer full		
	4	S_L0_THROTTLE	RO	State of the FE L0 throttle		
	5	S_DAQ_STPA	RO	State of the MAC FIFO full signal		
0AC	31 .. 0	C_EID_L	RO	L0 event ID (Bits 31 .. 0)		
0B0	31 .. 0	C_EID_H	RO	L0 Event ID (Bits 63 .. 032		
0B4	31 .. 0	C_GBE_FRAMES	RO	GbE frames transmitted		
0B8	8 .. 0	D_MB_WADDR	RO	Write address in MEP buffer		
0BC	8 .. 0	D_MB_RADDR	RO	Read address in MEP buffer		
0C0	8 .. 0	D_MB_LADDR	RO	Last write address in MEP buffer of previous MEP		
0E0		*READ_FEB*	RO	Read FEB buffer	Reading triggers a single read of the entire FEB	
0E4	31 .. 0	FEB_READ_0	RO	Front-End Buffer data in FEB 0/1		
0E8	31 .. 0	FEB_READ_1	RO	Frontt-End Buffer data in FEB 2/3		
0EC	31 .. 0	FEB_READ_2	RO	Front-End Buffer data in FEB 4/5		
0F0	31 .. 0	FEB_READ_3	RO	Front-End Buffer data in FEB 6/7		
0F4	0	TST_MODE		Set Q_FE in test mode		0
	1	TST_GBE_LOOPBACK_ENB		Set Q_FE in loopback test mode together with Q_L1		0
0F8	31 .. 0	TST_LBUS		Local bus test register		0
0FC	31 .. 0	VERSION	RO	Version number of the VHDL code	Date in decimal YEAR|MO|DA|HR	