

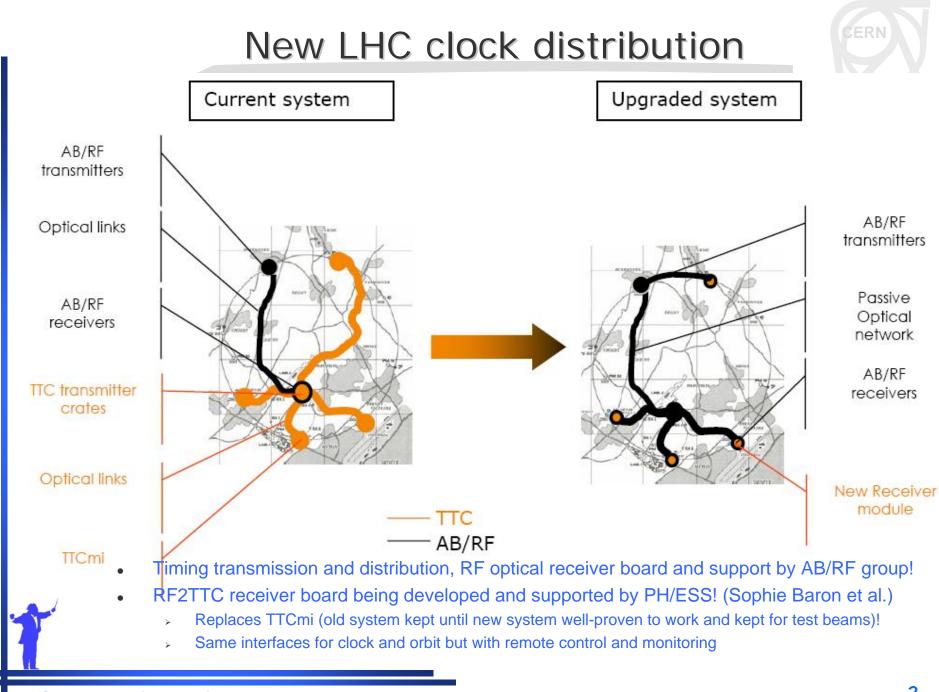


# LHC Clock Distribution & Monitoring Beam Phase and Intensity

- Already presented quality of timing clock stability and beam behaviour :
  - > December 2001
  - > May 2004 with proposal for a Beam Phase and Intensity Monitor (first design)
- Today: current status
  - > Up to know low-priority activity...

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LHCb week, Online meeting, November 29, 2005

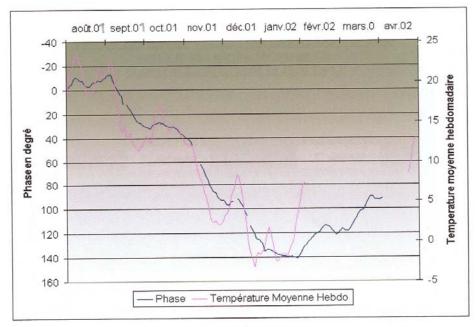


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# LHC Clock Phase Stability

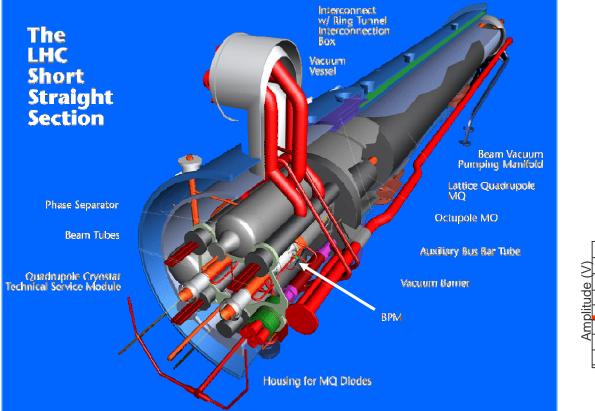


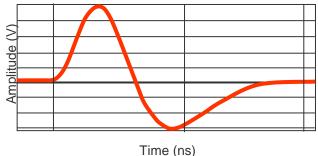
- Effect of temperature variations on distribution fibres
- Miss-management as I see it: we have lost the temperature-stabilized fibres between SR4 and CCC
- LHCb: 14.1 km of fibre between SR4 and PA8 at a depth of ~1m
  - Estimated max. diurnal drift 150 ps
  - Estimated max. seasonal drift 7ns



# Beam Monitoring at IP

#### >1000 Beam Position Monitors (BPMs) of the Button Electrode type





- Signal cables installed to TFC rack in counting rooms
  - > 1/2" Sucofeed corrugated 50-ohm coaxial cable
  - Peak voltage (one button) of ~5V after 200m of cable for nominal bunch
    - Sum voltage from all buttons → ~Independent of position

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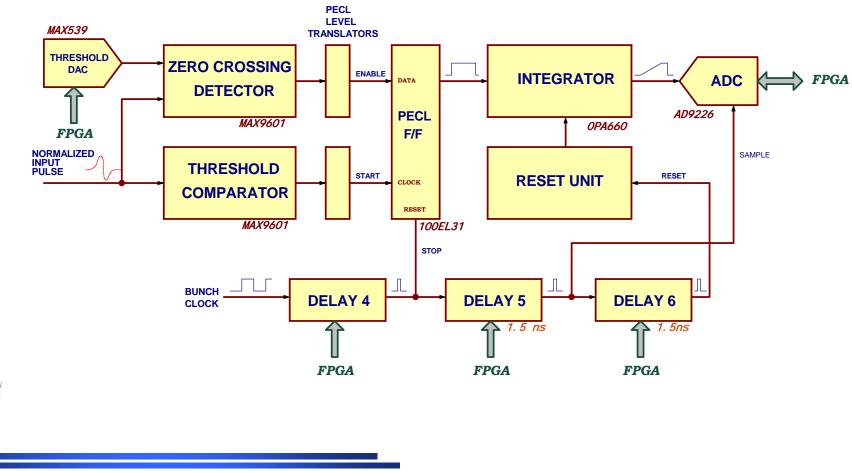


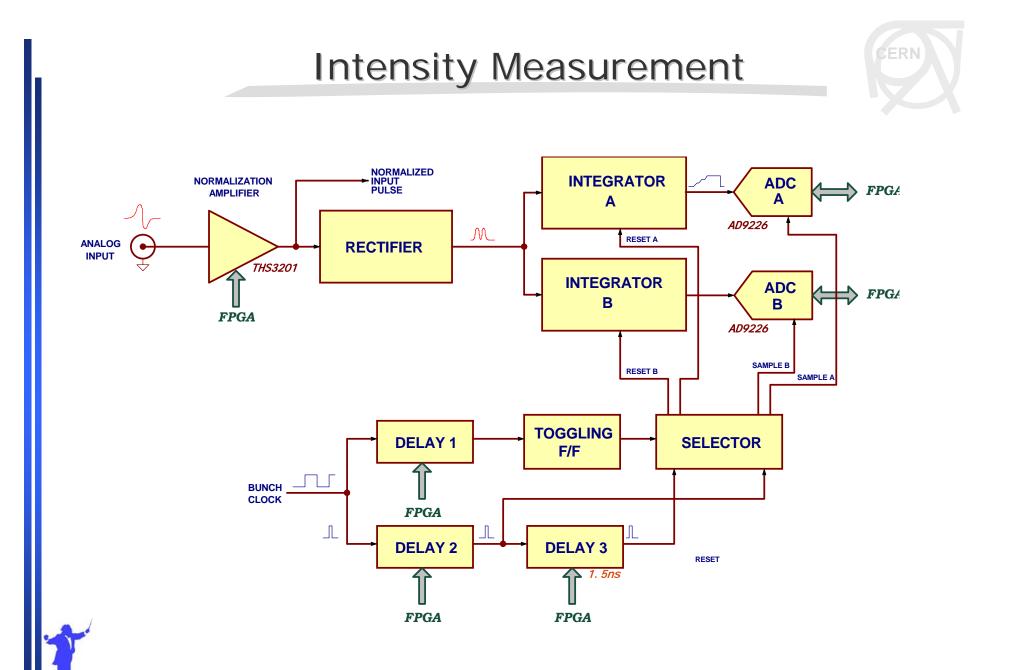
### LHCb Beam Phase and Intensity Monitor

- BPIM specifications:
  - Input signal processing:
    - Programmable amplification
    - Programmable threshold
  - Measuring beam intensity (~current)
    - Integrate pulse per bunch and averaging them
    - Resolution of intensity measurement 8 bits
    - Intensity per bunch as function of bunch crossing -> LHC bunch structure
    - Outputting intensity measurement at 40 MHz via LVDS interface
  - > Measuring phase between incoming bunch signal and bunch clock
    - Resolution of phase measurement ~50ps
    - Collecting phase measurement for every bunch and averaging them
    - Average phase per bunch crossing as function of bunch crossing
  - > Digital approximation of converter characteristics
  - Data processing in FPGA
  - CCPC based control interface
  - Board form-factor 6U or 9U?
    - Measure both beams on one board?

## Phase Measurement

- Revise the first design
  - Low-pass filter in LHC summing electronics
  - > Improve the design and more modern chips





# **BPIM Development**



#### • Design in progress

- > The entire analog part is in PSpice schematics
- Lot of simulation ahead
- > Digital part is relatively straight forward ("cut and paste"...)
- > Other activities in parallel
- > First tests can be done with existing beam pick-up emulator
- > Prototype will be connected up to real device on PS or SPS summer 2006 for tests