description

The 'LVT8980 embedded test-bus controllers (eTBC) are members of the TI broad family of testability integrated circuits. This family of devices supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit assemblies. Unlike most other devices of this family, the eTBC is not a boundary-scannable device; rather, its function is to master an IEEE Std 1149.1 (JTAG) test access port (TAP) under the command of an embedded host microprocessor/microcontroller. Thus, the eTBC enables the practical and effective use of the IEEE Std 1149.1 test-access infrastructure to support embedded/built-in test, emulation, and configuration/maintenance facilities at board and system levels.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
The eTBC masters all TAP signals required to support one 4- or 5-wire IEEE Std 1149.1 serial test bus – test clock (TCK), test mode select (TMS), test data input (TDI), test data output (TDO), and test reset (TRST). All such signals can be connected directly to the associated target IEEE Std 1149.1 devices without need for additional logic or buffering. However, as well as being directly connected, the TMS, TDI, and TDO signals can be connected to distant target IEEE Std 1149.1 devices via a pipeline, with a retiming delay of up to 15 TCK cycles; the eTBC automatically handles all associated serial-data justification.

Conceptually, the eTBC operates as a simple 8-bit memory- or I/O- mapped peripheral to a microprocessor/microcontroller (host). High-level commands and parallel data are passed to/from the eTBC via its generic host interface, which includes an 8-bit data bus (D7–D0) and a 3-bit address bus (A2–A0). Read/write select (R/W) and strobe (STRB) signals are implemented so that the critical host-interface timing is independent of the CLKIN period. An asynchronous ready (RDY) indicator is provided to hold off, or insert wait states into, a host read/write cycle when the eTBC cannot respond immediately to the requested read/write operation.

High-level commands are issued by the host to cause the eTBC to generate the TMS sequences necessary to move the test bus from any stable TAP-controller state to any other such stable state, to scan instruction or data through test registers in target devices, and/or to execute instructions in the Run-Test/Idle TAP state. A 32-bit counter can be programmed to allow a predetermined number of scan or execute cycles.

During scan operations, serial data that appears at the TDI input is transferred into a serial-to-4 × 8-bit-parallel first-in/first-out (FIFO) read buffer, which can then be read by the host to obtain the return serial-data stream up to eight bits at a time. Serial data that is to be transmitted from the TDO output is written by the host, up to eight bits at a time, to a 4 × 8-bit-parallel-to-serial FIFO write buffer.

In addition to such simple state-movement, scan, and run-test operations, the eTBC supports several additional commands that provide for input-only scans, output-only scans, recirculate scans (in which TDI is mirrored back to TDO), and a scan mode that generates the protocols used to support multidrop TAP configurations using TI’s addressable scan port. Two loopback modes also are supported that allow the microprocessor/microcontroller host to monitor the TDO or TMS data streams output by the eTBC.

The eTBC’s flexible clocking architecture allows the user to choose between free-running (in which the TCK always follows CLKIN) and gated modes (in which the TCK output is held static except during state-move, run-test, or scan cycles) as well as to divide down TCK from CLKIN. A discrete mode is also available in which the TAP is driven strictly by read/write cycles under full control of the microprocessor/microcontroller host. These features ensure that virtually any IEEE Std 1149.1 target device or device chain – even where such may not fully comply to IEEE Std 1149.1 – can be serviced by the eTBC.

While most operations of the eTBC are synchronous to CLKIN, a test-output enable (TOE) is provided for output control of the TAP outputs, and a reset (RST) input is provided for hardware reset of the eTBC. The former can be used to disable the eTBC so that an external controller can master the associated IEEE Std 1149.1 test bus.

The SN54LVT8980 is characterized for operation over the full military temperature range of $-55^\circ C$ to $125^\circ C$. The SN74LVT8980 is characterized for operation from $-40^\circ C$ to $85^\circ C$. 

The SN54LVT8980, SN74LVT8980
EMBEDDED TEST-BUS CONTROLLERS
IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES
functional block diagram

Pin numbers shown are for the DW and JT packages.
**Terminal Functions**

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2–A0</td>
<td>Address inputs. A2–A0 form the 3-bit address bus that interfaces the eTBC to its microprocessor/microcontroller host. These inputs directly index the eTBC register to be accessed (read from or written to).</td>
</tr>
<tr>
<td>CLkin</td>
<td>Clock input. CLkin is the system clock input for the eTBC. Most operations of the eTBC are synchronous to CLkin. Internally, the CLkin signal is divided by a programmable divisor to generate TCK.</td>
</tr>
<tr>
<td>D7–D0</td>
<td>Data inputs/outputs. D7–D0 form the 8-bit bidirectional data bus that interfaces the eTBC to its microprocessor/microcontroller host. Data in the eTBC registers is accessed (read or written) using this data bus. D7 is considered the most-significant bit, while D0 is considered the least-significant bit.</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>RDY</td>
<td>Ready output. RDY is used to indicate to the microprocessor/microcontroller host whether or not the eTBC is ready to service the access (read or write) operation that is currently being requested. If RDY remains high following the initiation of an access cycle (STRB negative edge) then the eTBC is ready. Otherwise, if RDY goes low following the initiation of an access cycle (STRB negative edge) then the eTBC is not ready. In cases where the eTBC is not ready, subsequent processing in the eTBC may clear the not-ready state, which allows RDY to return high before the end of the access cycle. In any event, the RDY output returns high upon the termination of any access cycle (STRB positive edge).</td>
</tr>
<tr>
<td>RST</td>
<td>Reset input. RST is used to initiate asynchronous reset of the eTBC. Assertion (low) of RST places the eTBC in a reset state from which it does not exit until RST is released (high). While RST is low, the eTBC ignores host writes, the RDY, TDO, TMS, and TRST outputs are high, while TCK outputs CLkin/16. An internal pullup forces RST to a high level if it has no external connection.</td>
</tr>
<tr>
<td>R/W</td>
<td>Read/write select. R/W is used by the microprocessor/microcontroller host to instruct the eTBC as to whether it is to perform read access (R/W high) or write access (R/W low). While R/W is high and STRB is low, the D7-D0 outputs are enabled to drive low and/or high logic levels onto the host data bus. Otherwise, while R/W is low, the D7–D0 outputs are disabled to a high-impedance state so that the host data bus can drive to the eTBC.</td>
</tr>
<tr>
<td>STRB</td>
<td>Read/write strobe. STRB is used by the microprocessor/microcontroller host to instruct the eTBC to initiate (STRB negative edge) or terminate/conclude (STRB positive edge) an access (read or write) operation. An internal pullup forces STRB to a high level if it has no external connection.</td>
</tr>
<tr>
<td>TCK</td>
<td>Test clock. TCK transmits the TCK signal required by the eTBC's IEEE Std 1149.1 target(s). All operations of the TAP are synchronous to TCK. Generally, the TCK signal is generated internally by the eTBC by division of CLkin by a programmable divisor. Alternatively, when the eTBC is in its discrete-control mode, a rising edge of TCK is generated on a read to the discrete-control register, while a falling edge is generated on a write to the discrete-control register.</td>
</tr>
<tr>
<td>TDI</td>
<td>Test data input. TDI receives the TDI signal output by the eTBC's IEEE Std 1149.1 target(s). It is the serial input for shifting test data from the target(s); it is sampled on the rising edge of TCK and is expected to be transferred from the target(s) on the falling edge of TCK. An internal pullup forces TDI to a high level if it has no external connection.</td>
</tr>
<tr>
<td>TDO</td>
<td>Test data output. TDO transmits the TDO signal required by the eTBC's IEEE Std 1149.1 target(s). It is the serial output for shifting test data to the target(s); it is transferred on the falling edge of TCK and is sampled in the target(s) on the rising edge of TCK.</td>
</tr>
<tr>
<td>TMS</td>
<td>Test mode select. TMS transmits the TMS signal required by the eTBC's IEEE Std 1149.1 target(s). It is the one control signal that directs the next TAP-controller state of the target(s). It is transferred from the eTBC on the falling edge of TCK and is sampled in the target(s) on the rising edge of TCK.</td>
</tr>
<tr>
<td>TOE</td>
<td>Test-output enable. TOE is the active-low output enable for the eTBC TAP outputs (TCK, TDO, TMS, TRST). When TOE is inactive (high) the TAP outputs are disabled to a high-impedance state. Otherwise, when TOE is active (low), the TAP outputs are enabled to drive low and/or high logic levels according to other eTBC functions. An internal pullup forces TOE to a high level if it has no external connection.</td>
</tr>
<tr>
<td>TRST</td>
<td>Test reset. TRST transmits the TRST signal that may be required by some of the eTBC's IEEE Std 1149.1 target(s). A low signal at TRST is intended to initiate asynchronous test reset of the connected target(s). Such a low signal at TRST is generated only when the microprocessor/microcontroller host writes an appropriate value into the eTBC command register or, while the eTBC is in discrete-control mode, into the discrete-control register.</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
</tr>
</tbody>
</table>
application information

In application, the eTBC is used to master a single IEEE Std 1149.1 TAP under the control of a microprocessor/microcontroller host. A typical implementation is shown in Figure 1.

All signals required to master IEEE Std 1149.1-compliant devices – TCK, TMS, TDO, TDI – are sourced/received by the eTBC. The eTBC can also source the optional TRST signal. Additionally, the eTBC implements high-drive output buffers, allowing it to interface directly to on- or off-board targets without need for buffering or other additional logic.

The eTBC’s generic host interface allows it to act as a simple 8-bit memory- or I/O-mapped peripheral. As shown in Figure 1, for many choices of host microprocessor/microcontroller, this interface can be accomplished without additional logic. While the eTBC requires a clock input (CLKIN), in many cases it can be driven from the same source that provides a clock signal to the host.

Thus, in combination with the host microprocessor/microcontroller, the eTBC can be used to implement a two-chip embedded test-control function supporting board- and system-level built-in test based on structured IEEE Std 1149.1 test access. In some cases, for additional program and/or test vector storage, an external ROM/RAM may be required.

By use of the eTBC in such an embedded test control function, the host microprocessor/microcontroller is freed from the burden of generating the TAP-state sequences, serializing the outgoing bit stream, and deserializing the incoming bit stream. All such tasks are implemented in the eTBC, allowing the host to operate at full 8-bit parallel efficiency, host software to operate at the level of discrete scan operations versus the level of TAP manipulation, and test throughput to be maximized. The eTBC’s full suite of data-scan and instruction-scan commands ensure that the host software operates efficiently.

Host efficiency and flexibility is also maximized through the eTBC’s fully visible status and implementation of the ready output (RDY). RDY goes inactive during a read or write access if the host-requested access cannot be performed immediately. Thus, it can be used to insert hold or wait states back to the host. When the condition blocking the access clears, the requested access completes. Additionally, all conditions that can cause such a blocking condition are continuously updated in the eTBC status and command registers. Thus, the host software can poll the eTBC status rather than implement RDY in hardware.
application information (continued)

The eTBC also provides several capabilities that support special target application requirements. The eTBC’s
test-output enable allows its master function to be disabled so that another device (an external tester, for
example) can control the target TAP. Where required, due to target non-compliance or sensitivity to state
sequencing, discrete-control mode provides the host software with arbitrary control of TMS and TDO
sequences. Also, where targets may be sensitive to leaving Shift-DR state during scan operation, gated-TCK
mode allows the TCK output to be stopped, rather than cycling the target TAP state to Pause-DR state, when
service to TDI buffer or TDO buffer is required.

Where target devices are extremely distant (due to cabling, etc.), pipelining may be implemented at intervals
along the incoming or outgoing paths to retime (deskew) the TDI, TDO, and TMS signals. An example is shown
in Figure 2. In such applications, the eTBC can automatically adjust the incoming test-data bit stream to account
for cycle delays introduced by the pipeline.

![Figure 2. Retimed Interface to Target](image)

Also, in gated-TCK mode, special scan commands provide transparent support for addressable shadow
protocols. Thus, in conjunction with its high-drive outputs, the eTBC can fully support multidrop backplane TAP
configurations implemented with TI’s addressable scan ports (ASP). Figure 3 shows a multidrop TAP
configuration in a passive-backplane application implemented with a centralized (one eTBC per chassis/rack)
test-control architecture, while Figure 4 shows a passive-backplane application implemented with a distributed
(eTBC per module) test-control architecture. Figure 5 shows a multidrop TAP configuration in an
active-backplane (motherboard) application.
Figure 3. Passive-Backplane Application With Centralized (eTBC Per Chassis) Test-Control Architecture
Figure 4. Passive-Backplane Application With Distributed Test-Control (eTBC Per Card) Architecture
architecture

Conceptually, the eTBC can be viewed as an IEEE Std 1149.1 coprocessor/accelerator that operates in conjunction with (and under the control of) a host microprocessor/microcontroller. The eTBC implements this function using an 8-bit generic host interface and a scan-test-based command/control architecture. As shown in the functional block diagram, beyond these fundamental elements and another central block supporting discrete-control mode, the eTBC functions are accomplished in four additional blocks – one for each of the required TAP signals – a TCK generator, a TAP-state (TMS) generator, a TDO buffer, and a TDI buffer.

host interface

The eTBC host interface is implemented generically on an 8-bit read/write data bus (D7–D0). Three address pins (A2–A0) directly index the eTBC’s eight read/write registers: configurationA, configurationB, status, command, TDO buffer, TDI buffer, counter, and discrete control. The register address map is given in Table 1.

host access timing

Host access timing is asynchronous to the clock input (CLKIN) and is fully controlled by the read/write strobe (STRB). The read/write select (R/W) serves to control the direction of data flow on the bidirectional data bus. Figure 6 shows the read access timing while Figure 7 shows the write access timing. As shown, for either read or write access, R/W and address signals should be held while STRB is low.

For read access (R/W high) the eTBC data bus outputs are made active, on the falling edge of STRB, to drive the data contained in the selected eTBC register. Otherwise, when STRB is high, the eTBC data outputs are at high impedance. Therefore, in many applications, the R/W signal can be shared in common with other host peripherals (ROM or RAM, for example) while the STRB signal is generated separately (by discrete chip-select signals available from the host or a decode logic) for each required peripheral.
host access timing (continued)

For write access (R/W low), the eTBC data outputs remain at high impedance independent of STRB. The address of the register to be written is latched from the address pins on the falling edge of STRB, while the data to be written is latched from the data bus on the rising edge of STRB.

**Figure 6. Read Access Timing**

**Figure 7. Write Access Timing**
ready output

The ready output (RDY) from the host interface can be used, where the selected microprocessor/microcontroller supports it, to insert wait or hold states back to the host. If a host-requested access cannot be performed immediately, RDY goes inactive (low) during that given access. When the condition blocking the access clears, RDY goes active (high) and the eTBC grants the requested access. Alternatively, where such hardware-generated hold or wait states are not supported in the selected microprocessor/microcontroller host, the eTBC status and/or command registers can be polled to determine its readiness to grant a given read or write access.

Conditions that cause a host access to be blocked (and RDY to become inactive) are limited to the following:

- While the TDI buffer is empty, as indicated in status register (bit 7, TDIS), a requested read to TDI-buffer register generates RDY inactive; this condition clears, RDY goes active, and the requested access completes, when the TDI buffer is no longer empty.

- While the TDO buffer is full or is being reset upon initiation of a scan command, as indicated in status register (bit 6, TDOS), a requested write to TDO-buffer register generates RDY inactive; this condition clears, RDY goes active, and the requested access completes, when the TDO buffer is no longer full or the TDO-buffer reset completes, as applicable.

- While a command is in progress, as indicated by a non-zero value in the opcode field (bits 3–0, OPCOD) of the command register, a requested write to command, configurationA, configurationB, or counter registers generates RDY inactive. This condition clears, RDY goes active, and the requested access is complete, when the previously specified command finishes. The sole exception is the writing of a logic 1 into the software reset (bit 7, SWRST) bit of the command register, which is never blocked.

- While a full-duplex scan command is in progress, and the number of retiming-delay bits is other than zero, the number of writes to TDO-buffer register may not exceed, by more than 5, the number of reads to TDI-buffer register. A write to TDO-buffer register that does exceed this limit is blocked, and generates RDY inactive, indefinitely; the TDI-buffer register must be read before another write to TDO-buffer register.
### register descriptions

A summary of the eTBC registers, their address mappings, bit assignments, reset values, and host accessibility (read/write or read-only) is provided in Table 1. All registers are fully readable by the host. All registers are fully writeable by the host with the exception of the status and TDI-buffer registers. Also, with the exception of TDO-buffer and command registers, writes to any register while a command is in progress are held off (RDY inactive) or ignored. Bits designated as reserved should be written to logic 0; read-only bits designated as reserved always read logic 0.

### Table 1. Register Summary

<table>
<thead>
<tr>
<th>ADDRESS A2–A0</th>
<th>REGISTER</th>
<th>REGISTER DETAIL (BIT ASSIGNMENTS)</th>
<th>RESET VALUE</th>
<th>HOST ACCESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>ConfigurationA</td>
<td>BIT 7 (MSB) BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0 (LSB)</td>
<td>0x00</td>
<td>R/W</td>
</tr>
<tr>
<td>001</td>
<td>ConfigurationB</td>
<td>BIT 7 (MSB) BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0 (LSB)</td>
<td>0x80</td>
<td>R/W</td>
</tr>
<tr>
<td>010</td>
<td>Status</td>
<td>BIT 7 (MSB) BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0 (LSB)</td>
<td>0x00</td>
<td>R</td>
</tr>
<tr>
<td>011</td>
<td>Command</td>
<td>BIT 7 (MSB) BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0 (LSB)</td>
<td>0x00</td>
<td>R/W</td>
</tr>
<tr>
<td>100</td>
<td>TDO buffer</td>
<td>BIT 7 (MSB) BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0 (LSB)</td>
<td>0x00</td>
<td>R/W</td>
</tr>
<tr>
<td>101</td>
<td>TDI buffer</td>
<td>BIT 7 (MSB) BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0 (LSB)</td>
<td>0x00</td>
<td>R</td>
</tr>
<tr>
<td>110</td>
<td>Counter</td>
<td>BIT 7 (MSB) BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0 (LSB)</td>
<td>0x00</td>
<td>R/W</td>
</tr>
<tr>
<td>111</td>
<td>Discrete control</td>
<td>BIT 7 (MSB) BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1 BIT 0 (LSB)</td>
<td>0x00</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### configuration registers

All eTBC test commands operate under the influence of the configurationA and configurationB registers. The decodes of the various bit groups assigned to these registers are given in Table 2 and Table 3, respectively. These registers are fully readable at all times and are fully writeable except when an eTBC command is in progress. Bit group values designated as reserved should not be written.
### Table 2. ConfigurationA Register Decode

<table>
<thead>
<tr>
<th>CONFIGURATIONA</th>
<th>BIT GROUP</th>
<th>VALUE</th>
<th>RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>nTOE</td>
<td>0</td>
<td>TAP outputs (TCK, TDO, TMS, TRST) are enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>TAP outputs (TCK, TDO, TMS, TRST) are disabled (high impedance).</td>
</tr>
<tr>
<td></td>
<td>LPBK</td>
<td>00</td>
<td>No loopback – TDI pin inputs to TDI buffer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
<td>TMS loopback – TAP-state generator inputs to TDI buffer. TMS and TDO pins are fixed high.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>TDO loopback – TDO buffer inputs to TDI buffer. TMS and TDO pins are fixed high.</td>
</tr>
<tr>
<td></td>
<td>MODE</td>
<td>000</td>
<td>Automatic/free-running-TCK mode – all TAP outputs are generated autonomously in the eTBC according to the active command. The TCK output runs continuously; while operating a scan command, if the TDI buffer becomes full and/or the TDO buffer becomes empty, the TAP state is cycled to Pause-DR or Pause-IR, as appropriate, until the host performs the required buffer service.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>001</td>
<td>Automatic/gated-TCK mode – all TAP outputs are generated autonomously in the eTBC according to the active command. The TCK output is run only when required to move TAP state to or progress run-test or scan operations, otherwise, it is gated off (low); while operating a scan command, if the TDI buffer becomes full and/or the TDO buffer becomes empty, the TAP state remains in Shift-IR or Shift-DR, as appropriate, but the TCK output is gated off until the host performs the required buffer service.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>010</td>
<td>Discrete-control mode – all TAP outputs are determined by contents of the discrete-control register under control of host software.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>011–111</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### Table 3. ConfigurationB Register Decode

<table>
<thead>
<tr>
<th>CONFIGURATIONB</th>
<th>BIT GROUP</th>
<th>VALUE</th>
<th>RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CDIV</td>
<td>000–111</td>
<td>TCK = (CLKIN)/(2^{CDIV}); reset value TCK = (CLKIN)/(2^4) = CLKIN/16</td>
</tr>
<tr>
<td></td>
<td>RDLY</td>
<td>0000–11</td>
<td>Number of retiming delays to accommodate = RDLY; while operating a scan command, TDI sampling is delayed by a number of TCK cycles, equal to RDLY, following the generation of Shift-DR or Shift-IR state, as appropriate.</td>
</tr>
</tbody>
</table>

The negated test-output-enable (nTOE) bit allows the host to disable the TAP outputs via software in a manner analogous to the hardware TOE. The loopback (LPBK) bit group allows the selection of the source of data to be input to the TDI buffer – from the TDI pin for normal eTBC operations or, for eTBC verification purpose, from TAP-state (TMS) generator or TDO buffer. The test mode (MODE) bit group provides a choice of automatic/free-running-TCK, automatic/gated-TCK, or discrete-control modes.

The clock-divisor (CDIV) bit group allows software control of the TCK output frequency based on a division of the CLKIN input. Divisors from 2^0 (1) to 2^7 (128) are provided. The clock divisor defaults to 2^4 (16) on eTBC reset (power-up, hardware-initiated, or software-initiated). The retiming-delay (RDLY) bit group provides for the automatic accommodation of retiming (pipeline) delays, which can be used to deskew the TAP signals to target scan chains that are electrically distant (due to cabling delays, etc).
status register

The status of the eTBC is fully reported and continuously updated in the status register. The decode of the various bit groups assigned to the status register is given in Table 4.

Table 4. Status Register Decode

<table>
<thead>
<tr>
<th>STATUS</th>
<th>VALUE</th>
<th>RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDIS 7</td>
<td>0</td>
<td>The TDI buffer is empty – no TDI data is available for host read.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The TDI buffer is not empty – at least one byte of TDI data is available for host read.</td>
</tr>
<tr>
<td>TDOS 6</td>
<td>0</td>
<td>The TDO buffer is not full – at least one byte in TDO buffer is available for host write.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The TDO buffer is full – no bytes in TDO buffer are available for host write.</td>
</tr>
<tr>
<td>CTRS 5</td>
<td>0</td>
<td>The counter is not loaded with a complete 32-bit value – command operation cannot begin until counter load completes.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The counter is loaded with a complete 32-bit value – command operation can begin.</td>
</tr>
<tr>
<td>TAPST 3-0</td>
<td>0000</td>
<td>The current target TAP state (as sent by eTBC) is Test-Logic-Reset.</td>
</tr>
<tr>
<td></td>
<td>0001</td>
<td>The current target TAP state (as sent by eTBC) is Select-DR-Scan.</td>
</tr>
<tr>
<td></td>
<td>0010</td>
<td>The current target TAP state (as sent by eTBC) is Capture-DR.</td>
</tr>
<tr>
<td></td>
<td>0011</td>
<td>The current target TAP state (as sent by eTBC) is Shift-DR.</td>
</tr>
<tr>
<td></td>
<td>0100</td>
<td>The current target TAP state (as sent by eTBC) is Exit1-DR.</td>
</tr>
<tr>
<td></td>
<td>0101</td>
<td>The current target TAP state (as sent by eTBC) is Pause-DR.</td>
</tr>
<tr>
<td></td>
<td>0110</td>
<td>The current target TAP state (as sent by eTBC) is Exit2-DR.</td>
</tr>
<tr>
<td></td>
<td>0111</td>
<td>The current target TAP state (as sent by eTBC) is Update-DR.</td>
</tr>
<tr>
<td></td>
<td>1000</td>
<td>The current target TAP state (as sent by eTBC) is Run-Test/Idle.</td>
</tr>
<tr>
<td></td>
<td>1001</td>
<td>The current target TAP state (as sent by eTBC) is Select-IR-Scan.</td>
</tr>
<tr>
<td></td>
<td>1010</td>
<td>The current target TAP state (as sent by eTBC) is Capture-IR.</td>
</tr>
<tr>
<td></td>
<td>1011</td>
<td>The current target TAP state (as sent by eTBC) is Shift-IR.</td>
</tr>
<tr>
<td></td>
<td>1100</td>
<td>The current target TAP state (as sent by eTBC) is Exit1-IR.</td>
</tr>
<tr>
<td></td>
<td>1101</td>
<td>The current target TAP state (as sent by eTBC) is Pause-IR.</td>
</tr>
<tr>
<td></td>
<td>1110</td>
<td>The current target TAP state (as sent by eTBC) is Exit2-IR.</td>
</tr>
<tr>
<td></td>
<td>1111</td>
<td>The current target TAP state (as sent by eTBC) is Update-IR.</td>
</tr>
</tbody>
</table>

The TDI-buffer-status (TDIS) bit reports the readiness of the TDI buffer to respond to a host read. The TDO-buffer-status (TDOS) bit reports the readiness of the TDO buffer to respond to a host write. The counter-status (CTRS) bit reports the readiness of the counter to support a command that uses the counter. The current-TAP-state (TAPST) bit group continuously reports the target TAP state as monitored by the eTBC.

command register

The command register is used to perform software reset of the eTBC, to discretely control the state of the TRST output when not in discrete-control mode, and to initiate test operations in the target(s). The decode of the various bits assigned to the command register is given in Table 5.

Any read to the command register while a command is in progress returns the value written to the command register upon initiation of the command. Once a command finishes, the operation-code (OPCOD) bit group in the command register is reset to null. In this way, the status of a requested command can be monitored/pollled by the host.

With the exception of the software-reset (SWRST) bit, which can be written at any time, writes to the command register while a command is in progress causes RDY inactive and is ignored if the write cycle is terminated before the previously requested command finishes.
## Table 5. Command Register Decode

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>BIT GROUP</th>
<th>BIT NO.</th>
<th>VALUE</th>
<th>RESULT</th>
<th>TEST OPERATION COMMENTS</th>
<th>WORKING TAP STATE</th>
<th>USES COUNTER</th>
<th>USES TDI BUFFER</th>
<th>USES TDO BUFFER</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWRST</td>
<td></td>
<td>7</td>
<td>0</td>
<td>Normal operation</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Full reset</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRST</td>
<td></td>
<td>6</td>
<td>0</td>
<td>If not in discrete-control mode, output high to TRST pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>If not in discrete-control mode, output low to TRST pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ENDST</td>
<td></td>
<td>5–4</td>
<td>00</td>
<td>Finish command in TAP state Test-Logic-Reset</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01</td>
<td>Finish command in TAP state Run-Test/Idle</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>Finish command in TAP state Pause-DR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11</td>
<td>Finish command in TAP state Pause-IR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPCOD</td>
<td>3–0</td>
<td>0000</td>
<td>Null</td>
<td>Run-Test/Idle</td>
<td></td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0001</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0010</td>
<td>Execute run test</td>
<td></td>
<td></td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0011</td>
<td>Execute input-only ASP scan</td>
<td></td>
<td></td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0100</td>
<td>Execute ASP scan</td>
<td></td>
<td></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0101</td>
<td>Execute output-only ASP scan</td>
<td></td>
<td></td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0110</td>
<td>Execute state move</td>
<td></td>
<td></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0111</td>
<td>Execute state jump</td>
<td></td>
<td></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000</td>
<td>Execute instruction-register scan</td>
<td></td>
<td></td>
<td>Shift-IR</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1001</td>
<td>Execute data-register scan</td>
<td></td>
<td></td>
<td>Shift-DR</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1010</td>
<td>Execute input-only instruction-register scan</td>
<td></td>
<td></td>
<td>Shift-IR</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1011</td>
<td>Execute input-only data-register scan</td>
<td></td>
<td></td>
<td>Shift-DR</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1100</td>
<td>Execute output-only instruction-register scan</td>
<td></td>
<td></td>
<td>Shift-IR</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1101</td>
<td>Execute output-only data-register scan</td>
<td></td>
<td></td>
<td>Shift-DR</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1110</td>
<td>Execute recirculate instruction-register scan</td>
<td></td>
<td></td>
<td>Shift-IR</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1111</td>
<td>Execute recirculate data-register scan</td>
<td></td>
<td></td>
<td>Shift-DR</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

The software-reset (SWRST) bit is provided to allow software initiation of full eTBC reset. This bit of the command register can be written at any time, regardless of the configuration or command in progress. The test-reset (TRST) bit allows direct software control of the state of TRST output in modes other than discrete control.

The end-TAP-state (ENDST) bit group determines the TAP state in which the target scan chain is left when the requested command finishes. The operation-code (OPCOD) bit group determines the test operation to be executed in the target.
counter register

The counter register, while only 8 bits wide like any other eTBC register, provides read/write access to the full 32-bit eTBC counter. Writes to the counter register are accomplished by four complete host access cycles, otherwise the counter is considered unloaded (CTRS = 0). Reads to the counter register likewise are accomplished by four complete host access cycles. However, reads do not affect the counter-loaded status (CTRS). The counter access (both read and write) is in least-significant-byte-first order. Any writes to the counter register while a command is in progress are ignored. The 32-bit value present in the counter at initiation of a command is used to determine the number of TCK cycles or scan bits for which the command is operated.

TDO-buffer register

The TDO-buffer register, while only 8 bits wide like any other eTBC register, provides write access to the full $4 \times 8$ (32-bit) FIFO that comprises the TDO buffer. The TDO-buffer register can be written as long as the TDO buffer does not become full. When the TDO buffer becomes full, further writes to the TDO-buffer register cause RDY inactive (and consequent hold or wait states to be sent back to the host, if supported) and cause the write to be ignored if the write cycle is terminated before the TDO-buffer-full status is cleared.

TDI-buffer register

The TDI-buffer register, while only 8 bits wide like any other eTBC register, provides read access to the full $4 \times 8$ (32-bit) FIFO that comprises the TDI buffer. The TDI-buffer register can be read as long as the TDI buffer does not become empty. When the TDI buffer becomes empty, further reads to the TDI-buffer register cause RDY inactive (and consequent hold or wait states to be sent back to the host, if supported) and cause the read data to be invalid if the read cycle is terminated before the TDI-buffer-empty status is cleared.

discrete-control register

The discrete-control register is used to program the state of the TAP outputs (TCK, TDO, TMS, TRST) and to poll the state of the TAP input (TDI) when the eTBC is in its discrete-control mode. The contents of the discrete-control register determine values output to TDO, TMS, and TRST according to the decode in Table 6. The TCK output is generated on each read and write to the discrete-control register; writes generate TCK falling edge, while reads generate TCK rising edge. In modes other than the discrete-control mode, this register is fully writeable and readable, but writes and reads have no effect on eTBC or target operation.

<table>
<thead>
<tr>
<th>DISCRETE CONTROL</th>
<th>VALUE</th>
<th>RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DNTR 3</td>
<td>0</td>
<td>If in discrete-control mode, output low to TRST pin, otherwise nothing</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>If in discrete-control mode, output high to TRST pin, otherwise nothing</td>
</tr>
<tr>
<td>DTMS 2</td>
<td>0</td>
<td>If in discrete-control mode, output low to TMS pin, otherwise nothing</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>If in discrete-control mode, output high to TMS pin, otherwise nothing</td>
</tr>
<tr>
<td>DTDI 1</td>
<td>0</td>
<td>The TDI data received is a logic 0.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The TDI data received is a logic 1.</td>
</tr>
<tr>
<td>DTDO 0</td>
<td>0</td>
<td>If in discrete-control mode, output low to TDO pin, otherwise nothing</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>If in discrete-control mode, output high to TDO pin, otherwise nothing</td>
</tr>
</tbody>
</table>
command/control

The eTBC’s command-based architecture is structured around a set of comprehensive IEEE Std 1149.1 (JTAG) test objectives, which include TAP state movement, scan operations, and run test (operation of test logic in Run-Test/Idle state). The set of test operations, as decoded from the command register (bits 3–0, OPCOD) is given in Table 5. Commands are initiated by writing the eTBC command register; upon command initiation, the test-control logic is initialized and the TDO and TDI buffers are cleared. Command completion is indicated when the operation code (OPCOD) field of the command register returns to the value of the null command.

The eTBC command operation is modified by the configurationA, and configurationB registers, which should be written prior to writing the command register, as the values in these registers cannot be modified while a command is in progress. Also, commands are only operated in automatic test modes, as specified in the configurationA register (bits 2–0, MODE) – while in the discrete-control mode, commands are ignored.

All eTBC commands operate similarly to accomplish IEEE Std 1149.1 test objectives. First, the eTBC generates a TMS sequence to move the target scan chain from its current TAP state to a working state that depends on the test objective. Second, the command is operated (test run, bits scanned) in the working state for a number of TCK cycles (or scan bits) determined by the value of the counter upon command initiation. Third, the eTBC generates a TMS sequence to move the target scan chain from the working state to the end state specified in the command register (bits 5–4, ENDST). For some commands, one or more of these steps are omitted.

TAP-state-movement commands

Two eTBC commands are provided to accomplish TAP state movement. The state-move command operates to generate a TMS sequence to move the target scan chain directly from its current TAP state to the end state specified in the command register. The state-jump command moves the eTBC’s stored value of the target TAP state without generating any changes to the TMS output. The state-jump command can therefore be used to switch between targets that share the same test bus, such as those in a multidrop backplane configuration implemented with TI addressable scan ports, but that may be left in different TAP states.

run-test command

The run-test command allows the test logic of the target scan chain to execute autonomously in the Run-Test/Idle TAP state. Such test logic is commonly used to implement chip- or board-level built-in self test. The run-test command generates TMS sequences to move the target scan chain from its current TAP state to the Run-Test/Idle TAP state where it remains for a number of TCK cycles determined by the value of the counter upon command initiation. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

scan commands

Eleven eTBC commands are provided to perform scan operations to target scan chains. These can be classified by the destination of scan data in the target – addressable scan port (ASP), IEEE Std 1149.1 instruction register, or IEEE Std 1149.1 data register – and by the nature/direction of the data transfer – full-duplex (default), input-only, output-only, or recirculate. The only combination of these two factors that is not implemented is recirculate ASP scan.

addressable scan port (ASP) scan commands

The ASP scan commands scan data to and/or from an addressable scan port target. Since ASP devices require that TMS remain fixed throughout their select and acknowledge protocols, the eTBC does not generate TMS sequences or change its stored value of the target’s TAP state. Also, for the same reason, ASP scan commands that target ASP devices should be operated in gated-TCK mode. The ASP scan commands do allow data written to the TDO buffer to be driven serially onto the TDO pin and bits received serially at the TDI pin to be stored into the TDI buffer for reading by the host. However, the ASP scan commands do not perform any bit-pair encoding of ASP select protocols or decoding of ASP acknowledge protocols. Such encoding/decoding must be performed in the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation.
The instruction-register scan commands scan bits to and/or from the concatenation of instruction registers in a target scan chain. The eTBC generates a TMS sequence to move the target scan chain from its current TAP state to the Shift-IR TAP state. Data written to the TDO buffer can be driven serially onto the TDO pin and bits received serially at the TDI pin can be stored into the TDI buffer for reading by the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation. If, during the operation of an instruction register scan command, the TDO buffer becomes empty, or the TDI buffer becomes full, the TAP state is sequenced to Pause-IR (if in free-running-TCK mode) or the TCK output is gated off (if in gated-TCK mode) until the required buffer service is performed. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

The data-register scan commands operate to scan bits to and/or from the concatenation of data registers in a target scan chain. The eTBC generates a TMS sequence to move the target scan chain from its current TAP state to the Shift-DR TAP state. Data written to the TDO buffer may be driven serially onto the TDO pin and bits received serially at the TDI pin may be stored into the TDI buffer for reading by the host. The number of data bits transferred in and/or out is determined by the value of the counter upon command initiation. If, during the operation of a data-register scan command, the TDO buffer becomes empty, or the TDI buffer becomes full, the TAP state is sequenced to Pause-DR (if in free-running-TCK mode) or the TCK output is gated off (if in gated-TCK mode) until the required buffer service is performed. Upon the countdown of the counter to zero, the eTBC generates TMS sequences to move the target scan chain to the end state specified in the command register.

As noted before, the nature/direction of the data transfer for any scan command can vary along with the destination of scan data in the target, as follows:

- For scan commands of the full-duplex (default) class, both TDO buffer and TDI buffer are used to scan data to and from the target scan chain, respectively.
- For scan commands of the input-only class, only the TDI buffer is used to scan data from the target scan chain; outgoing TDO data is fixed at a high level throughout the scan operation.
- For scan commands of the output-only class, only the TDO buffer is used to scan data to the target scan chain; incoming TDI data is simply ignored.
- For scan commands of the recirculate class, only the TDI buffer is used to scan data from the target scan chain; outgoing TDO data is generated by recirculating the incoming TDI data back into the target scan chain.

As described above, the value loaded in the eTBC’s 32-bit counter at initiation of a command is used to specify the number of TCK cycles or scan bits to remain in the command’s working state. As each TCK cycle or scan bit is processed for a run-test or scan command, respectively, the counter value is decremented. When the counter value reaches zero, the command leaves its working state to finish in the end state specified in the command register.

Before a command that uses the counter can be initiated, a full 32-bit value should be loaded by four consecutive writes to the counter register. As well, the full 32-bit current value of the counter can be observed by four consecutive reads to the counter register. The counter status (unloaded/loaded) is maintained and observable in the status register (bit 5, CTRS).

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the counter is cleared and assumes its unloaded state.
TCK generator

The TCK generator sources the test clock (TCK) signal required by the IEEE Std 1149.1 target(s) and the eTBC-internal test-control logic. The fundamental TCK frequency is produced by division of CLKIN. The divisor is programmable within a range of 1 to 128 in the configurationB register (bits 7–5, CDIV). The TCK output to the target(s) operate in free-running or gated modes. The free-running mode toggles TCK continuously, based on CLKIN, while the gated mode operates the TCK only when required to move the target TAP state or to perform a run-test or scan operation.

While the eTBC is in discrete-control mode, the TCK generator is not used; instead, the state of TCK is toggled on each alternating read and write to the discrete-control register. A falling edge of TCK is produced by write, while a rising edge of TCK is produced by read.

Upon eTBC reset (power-up, hardware-initiated, or software-initiated), the TCK generator assumes its free-running mode with a clock divisor of 16 (TCK = CLKIN/16).

TAP-state generator

The TAP-state generator sources the TMS signal, which sequences the TAP controllers of connected IEEE Std 1149.1-compliant target devices. The TAP controller specified by IEEE Std 1149.1 is a synchronous finite-state machine that provides test control signals throughout each target device; its state diagram is shown in Figure 8. This diagram and the TAP-controller states are discussed subsequently.

The TAP-state generator operates under the control of an executing command to generate the TMS sequences required to move connected target devices from one stable state to another, to capture and scan test data into/out of target devices, and to operate built-in test modes of target devices in the Run-Test/Idle state.

The TAP state currently being generated is always maintained by the TAP-state generator and is constantly available in the eTBC status register (bits 3–0, TAPST) for host read. Based on the TAP state that is current upon command initiation, the TAP-state generator will source a defined sequence of TMS values to reach the TAP state in which the command is progressed (e.g., Shift-IR, Shift-DR, Run-Test/Idle), and ultimately to reach the specified end TAP state. These sequences are detailed in Tables 7–12.

While the eTBC is in free-running-TCK mode, if a currently operating scan command empties or fills a required test data buffer, then the TAP-state generator sources the TMS sequences required to move the connected target devices to their Pause-IR or Pause-DR states. In such case, the TAP-state generator maintains target devices in their Pause-IR or Pause-DR states until the required test data buffer is serviced appropriately. However, if such a buffer condition occurs while the eTBC is in gated-TCK mode, the TAP-state generator maintains the target devices in their Shift-IR or Shift-DR states while the TCK is gated off.

While the eTBC is in discrete-control mode, the TAP-state generator is not used; instead, the state of the TMS pin is determined by the contents of the discrete-control register. Thus, TMS sequences that cannot be generated automatically still can be applied through the eTBC to targets that require such (e.g., near-compliant devices).

The TAP-state generator also is not used during the operation of the special addressable shadow protocol (ASP) scan commands. Since, by definition, ASPs operate only while the TAP is idling (maintaining one of the TAP states Test-Logic-Reset, Run-Test/Idle, Pause-IR, or Pause-DR), the TMS pin must be maintained at the value it held upon initiation of the ASP scan command.

For eTBC verification/debugging, in addition to continuous update of the current target TAP state in the eTBC status register, the output of the TAP-state (TMS) generator can be selected for loopback into the TDI buffer. When this TMS-loopback mode is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TAP-state generator assumes the Test-Logic-Reset TAP state.
### Table 7. TMS Sequencing From TAP State Test-Logic-Reset

<table>
<thead>
<tr>
<th>FROM TEST-LOGIC-RESET (TMS = H) TO:</th>
<th>TEST-LOGIC-RESET</th>
<th>RUN-TEST-IDLE</th>
<th>SHIFT-DR</th>
<th>PAUSE-DR</th>
<th>SHIFT-IR</th>
<th>PAUSE-IR</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
</tr>
<tr>
<td>H</td>
<td>T-L-R</td>
<td>L</td>
<td>R-T/I</td>
<td>L</td>
<td>R-T/I</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>S-DR-S</td>
<td>H</td>
<td>S-DR-S</td>
<td>H</td>
<td>S-DR-S</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>Capture-DR</td>
<td>L</td>
<td>Capture-DR</td>
<td>H</td>
<td>S-IR-S</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>Shift-DR</td>
<td>H</td>
<td>Exit1-DR</td>
<td>L</td>
<td>Capture-IR</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>Pause-DR</td>
<td>L</td>
</tr>
</tbody>
</table>

### Table 8. TMS Sequencing From TAP State Run-Test/Idle

<table>
<thead>
<tr>
<th>FROM RUN-TEST/IDLE (TMS = L) TO:</th>
<th>TEST-LOGIC-RESET</th>
<th>RUN-TEST-IDLE</th>
<th>SHIFT-DR</th>
<th>PAUSE-DR</th>
<th>SHIFT-IR</th>
<th>PAUSE-IR</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
</tr>
<tr>
<td>H</td>
<td>S-DR-S</td>
<td>L</td>
<td>R-T/I</td>
<td>H</td>
<td>S-DR-S</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>S-IR-S</td>
<td>L</td>
<td>Capture-DR</td>
<td>L</td>
<td>Capture-DR</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>T-L-R</td>
<td>L</td>
<td>Shift-DR</td>
<td>H</td>
<td>Exit1-DR</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>Pause-DR</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
</tr>
</tbody>
</table>

### Table 9. TMS Sequencing From TAP State Pause-DR

<table>
<thead>
<tr>
<th>FROM PAUSE-DR (TMS = L) TO:</th>
<th>TEST-LOGIC-RESET</th>
<th>RUN-TEST-IDLE</th>
<th>SHIFT-DR</th>
<th>PAUSE-DR</th>
<th>SHIFT-IR</th>
<th>PAUSE-IR</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
</tr>
<tr>
<td>H</td>
<td>Exit2-DR</td>
<td>H</td>
<td>Exit2-DR</td>
<td>H</td>
<td>Exit2-DR</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>Update-DR</td>
<td>H</td>
<td>Update-DR</td>
<td>L</td>
<td>Shift-DR</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>S-DR-S</td>
<td>L</td>
<td>R-T/I</td>
<td>H</td>
<td>S-DR-S</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>S-IR-S</td>
<td>L</td>
<td>Capture-DR</td>
<td>H</td>
<td>S-IR-S</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>T-L-R</td>
<td>L</td>
<td>Exit1-DR</td>
<td>L</td>
<td>Capture-IR</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
<td>Pause-DR</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L</td>
</tr>
</tbody>
</table>
Table 10. TMS Sequencing From TAP State Pause-IR

<table>
<thead>
<tr>
<th>FROM PAUSE-IR (TMS = L) TO:</th>
<th>TEST-LOGIC-RESET</th>
<th>RUN-TEST-IDLE</th>
<th>SHIFT-DR</th>
<th>PAUSE-DR</th>
<th>SHIFT-IR</th>
<th>PAUSE-IR</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
</tr>
<tr>
<td>H</td>
<td>Exit2-IR</td>
<td>H</td>
<td>Exit2-IR</td>
<td>H</td>
<td>Exit2-IR</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>Update-IR</td>
<td>H</td>
<td>Update-IR</td>
<td>H</td>
<td>Update-IR</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>S-DR-S</td>
<td>L</td>
<td>R-T/I</td>
<td>H</td>
<td>S-DR-S</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>T-L-R</td>
<td>L</td>
<td>Shift-DR</td>
<td>H</td>
<td>Exit1-DR</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 11. TMS Sequencing From TAP State Shift-DR

<table>
<thead>
<tr>
<th>FROM SHIFT-DR (TMS = L) TO:</th>
<th>TEST-LOGIC-RESET</th>
<th>RUN-TEST-IDLE</th>
<th>PAUSE-DR</th>
<th>PAUSE-IR</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
</tr>
<tr>
<td>H</td>
<td>Exit1-DR</td>
<td>H</td>
<td>Exit1-DR</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>Update-DR</td>
<td>H</td>
<td>Update-DR</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>S-DR-S</td>
<td>L</td>
<td>R-T/I</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>T-L-R</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 12. TMS Sequencing From TAP State Shift-IR

<table>
<thead>
<tr>
<th>FROM SHIFT-IR (TMS = L) TO:</th>
<th>TEST-LOGIC-RESET</th>
<th>RUN-TEST-IDLE</th>
<th>PAUSE-DR</th>
<th>PAUSE-IR</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
<td>NEXT TAP STATE</td>
<td>NEXT TMS</td>
</tr>
<tr>
<td>H</td>
<td>Exit1-IR</td>
<td>H</td>
<td>Exit1-IR</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>Update-IR</td>
<td>H</td>
<td>Update-IR</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>S-DR-S</td>
<td>L</td>
<td>R-T/I</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>S-IR-S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>T-L-R</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
state diagram description

The state diagram shown in Figure 8 is in accordance with IEEE Std 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at any given time.

![Figure 8. TAP-Controller State Diagram](image-url)
Test-Logic-Reset

The eTBC TAP-state generator powers up in the Test-Logic-Reset state. Alternatively, the eTBC can be forced to this state asynchronously by assertion of its RST input or synchronously by writing the eTBC command register (bit 7-SWRST).

For a target device in the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

Run-Test/Idle

For a target device, Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

Select-DR-Scan, Select-IR-Scan

For a target device, no specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

Capture-DR

For a target device in the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the Capture-DR state is exited.

Shift-DR

For a target device, upon entry to the Shift-DR state, the selected data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the selected data register. While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle.

Exit1-DR, Exit2-DR

For a target device, the Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

For target devices, no specific function is performed in the stable Pause-DR state. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

Update-DR

For a target device, if the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

Capture-IR

For a target device in the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the Capture-IR state is exited.
Shift-IR

For a target device, upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO outputs the logic level present in the least-significant bit of the instruction register. While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle.

Exit1-IR, Exit2-IR

For target devices, the Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

For target devices, no specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

Update-IR

For target devices, the current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

TDO buffer

The TDO buffer is the $4 \times 8$-bit-parallel-to-serial FIFO that accepts scan data from the host in 8-bit-parallel format and serializes it onto the TDO pin during scan operations. Scan data is expected to be transferred from the host in least-significant-byte-first order to meet IEEE Std 1149.1 requirements for least-significant-bit-first scan order. Any partial byte to be written should be justified to D0. The TDO buffer is cleared upon command initiation, so no scan data should be written to the TDO buffer before writing a scan command to the command register.

The TDO-buffer status (not full/full) is maintained in the status register (bit 6, TDOS). When the TDO-buffer status is full, writes to the TDO buffer is held off by RDY inactive and if the write cycle is aborted prior to RDY active, the write data is ignored.

For the convenience and efficiency of operating scans to the target for which outgoing data is not required, the eTBC supports special classes of input-only and recirculate scan commands that do not require nor operate the TDO buffer and so the host need not perform any write access to it. While the input-only scan commands are operating, the TDO pin outputs a fixed high level. While the recirculate scan commands are operating, the TDO pin recirculates to the target the data that is received at TDI.

While the eTBC is in discrete-control mode, the TDO buffer is not used; instead, the state of the TDO pin is determined by the contents of the discrete-control register. Thus, TMS/TDO sequences that cannot be automatically generated still can be applied through the eTBC to targets that require such (e.g., near-compliant devices).

For eTBC verification/debugging, the TDO-buffer output can be selected for loopback into the TDI buffer. When this TDO-loopback mode is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TDO buffer is cleared and assumes its not-full state.
TDI buffer

The TDI buffer is the serial-to-4 × 8-bit-parallel FIFO that serially receives data at the TDI pin and makes it available in 8-bit-parallel format for reading by the host. Scan data is expected to be transferred from the IEEE Std 1149.1 targets in least-significant-bit-first order and is made available for host read in least-significant-byte-first order. The last data available for host read during a scan command may be a partial byte, in which case it is justified to D0.

The TDI-buffer status (empty/not empty) is maintained in the status register (bit 7, TDIS). When the TDI-buffer status is empty, reads to the TDI buffer is held off by RDY inactive and, if the read cycle is aborted prior to RDY active, the read data is invalid.

The TDI buffer is able to automatically accommodate retiming (pipeline) delays to the target. While operating a scan command, TDI sampling is delayed by a number of TCK cycles, equal to a value given in the configurationB register (bits 3–0, RDLY), following the generation of Shift-DR or Shift-IR state, as appropriate.

For the convenience and efficiency of operating scans to the target for which incoming data is not required, the eTBC supports a special class of output-only scan commands that neither require nor operate the TDI buffer. While the output-only scan commands are operating, the data received at TDI is ignored and the host need not perform any read access to the TDI buffer.

While the eTBC is in discrete-control mode, the TDI buffer is not used; instead, the state of the TDO pin is observed in the discrete-control register. Thus, TMS/TDO sequences that cannot be automatically generated can still be applied through the eTBC to targets that require such (e.g., near-compliant devices).

For eTBC verification/debugging, the input to the TDI buffer can be selected for loopback from either TDO buffer or TAP-state (TMS) generator. When either of these loopback modes is selected, although a host-requested command executes in the eTBC, the target is not affected, as both TMS and TDI are fixed at a high level.

Upon eTBC reset (power up, hardware initiated, or software initiated), the TDI buffer is cleared and assumes its empty state.

discrete control

The discrete-control block provides the multiplexing and control logic required to support the eTBC’s discrete-control mode in addition to its automatic modes. While the eTBC is in discrete-control mode, the TAP signals are fully controllable/accessible to the host via reads/writes to the discrete-control register. No commands can be initiated/operated while the eTBC is in the discrete-control mode.

Upon eTBC reset (power up, hardware initiated, or software initiated), the discrete-control mode is inactive.

reset

The eTBC provides three mechanisms for comprehensive and equivalent reset – power-up reset, hardware-initiated reset (RST), and software-initiated reset (SWRST, bit 7 of command register) to the following effect:

- All eTBC registers are reset to default values as given in Table 1.
- The command/control logic is fully reset.
- The counter is cleared/unloaded. The TDO buffer and TDI buffer are cleared/emptied.
- The TAP-state generator is reset to the Test-Logic-Reset TAP state.
- TDO, TMS, and TRST output high levels; TCK outputs CLKIN/16.

As a consequence, the IEEE Std 1149.1 targets can be expected to be driven synchronously to the Test-Logic-Reset state no later than the fifth rising edge of TCK (72 CLKIN cycles).
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, \( V_{CC} \) .............................................................. –0.5 V to 4.6 V
Input voltage range, \( V_I \) (see Note 1) ...................................................... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, \( V_O \)
(see Note 1): D, RDY .............................................................. –0.5 V to \( V_{CC} + 0.5 V \)
TCK, TDO, TMS, TRST .............................................................. –0.5 V to 7 V
Current into any output in the low state, \( I_O \):
SN54LVT8980 (D, RDY) .............................................................. 12 mA
SN54LVT8980 (TCK, TDO, TMS, TRST) .................................................. 96 mA
SN74LVT8980 (D, RDY) .............................................................. 12 mA
SN74LVT8980 (TCK, TDO, TMS, TRST) .................................................. 128 mA
Current into any output in the high state, \( I_O \)
(see Note 2): SN54LVT8980 (D, RDY) .............................................................. 16 mA
SN54LVT8980 (TCK, TDO, TMS, TRST) .................................................. 48 mA
SN74LVT8980 (D, RDY) .............................................................. 16 mA
SN74LVT8980 (TCK, TDO, TMS, TRST) .................................................. 64 mA
Input clamp current, \( I_{IK} \) (\( V_I < 0 \)) ...................................................... –50 mA
Output clamp current, \( I_{OK} \) (\( V_O < 0 \)) ...................................................... –50 mA
Output clamp current, \( I_{OK} \) (\( V_O > V_{CC} \)): D, RDY ...................................................... 50 mA
Package thermal impedance, \( \theta_{JA} \) (see Note 3): DW package ...................................................... 81°C/W
Storage temperature range, \( T_{stg} \) .............................................................. –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This current flows only when the output is in the high state and \( V_O > V_{CC} \).
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54LVT8980</th>
<th>SN74LVT8980</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>MAX</td>
</tr>
<tr>
<td>( V_{CC} ) Supply voltage</td>
<td>2.7</td>
<td>3.6</td>
</tr>
<tr>
<td>( V_{IH} ) High-level input voltage</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>( V_{IL} ) Low-level input voltage</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>( V_I ) Input voltage</td>
<td>5.5</td>
<td>5.5</td>
</tr>
<tr>
<td>( I_{OH} ) High-level output current</td>
<td>D, RDY</td>
<td>–8</td>
</tr>
<tr>
<td></td>
<td>TCK, TDO, TMS, TRST</td>
<td>–24</td>
</tr>
<tr>
<td>( I_{OL} ) Low-level output current</td>
<td>D, RDY</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>TCK, TDO, TMS, TRST</td>
<td>48</td>
</tr>
<tr>
<td>( \Delta t/\Delta v ) Input transition rise or fall rate</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>( \Delta t/\Delta V_{CC} ) Power-up ramp rate</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>( T_A ) Operating free-air temperature</td>
<td>–55</td>
<td>125</td>
</tr>
</tbody>
</table>

NOTE 4: Unused control inputs (A, CLKIN, R/W) must be held high or low to prevent them from floating.
**SN54LVT8980, SN74LVT8980**  
**EMBEDDED TEST-BUS CONTROLLERS**  
**IEEE STD 1149.1 (JTAG) TAP MASTERS WITH 8-BIT GENERIC HOST INTERFACES**  

---

## Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SN54LVT8980</th>
<th>SN74LVT8980</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>V(\text{IL})</strong></td>
<td>(V_{CC} = 2.7) (V), (I_{\text{I}} = -18) mA</td>
<td>MIN: –1.2</td>
<td>TYP(\dagger): –1.2</td>
<td>(V)</td>
</tr>
<tr>
<td><strong>V(\text{OH})</strong></td>
<td>(V_{CC} = \text{MIN to MAX}^{\ddagger}), (I_{\text{OH}} = -100) (\mu)A</td>
<td>V(\text{CC}) –0.2</td>
<td>V(\text{CC}) –0.2</td>
<td>(V)</td>
</tr>
<tr>
<td><strong>D, RDY</strong></td>
<td>(V_{CC} = 3) (V)</td>
<td>(I_{\text{OH}} = -4) mA</td>
<td>(I_{\text{OH}} = -8) mA</td>
<td>2.6</td>
</tr>
<tr>
<td><strong>TCK, TDO, TMS, TRST</strong></td>
<td>(V_{CC} = 2.7) (V), (I_{\text{OH}} = -8) mA</td>
<td>(I_{\text{OH}} = -24) mA</td>
<td>2</td>
<td>(I_{\text{OH}} = -32) mA</td>
</tr>
</tbody>
</table>

| **IOH** | \(V_{CC} = \text{MIN to MAX}^{\ddagger}\), \(I_{\text{OH}} = 100\) \(\mu\)A | 0.2 | 0.2 | \(V\) |
| **IOL** | \(V_{CC} = 0\) or \(\text{MAX}^{\ddagger}\), \(V_{I} = 5.5\) \(V\) | 10 | 10 | \(\mu\)A |
| **I\(\text{off}\)** | \(V_{CC} = 0\), \(V_{I} = 0\) to 4.5 \(V\) | \(\pm 100\) | \(\pm 100\) | \(\mu\)A |
| **I\(\text{OZH}\)** | \(V_{CC} = 3.6\) \(V\), \(V_{O} = 0\) to 3 \(V\) | 5 | 5 | \(\mu\)A |
| **I\(\text{OZL}\)** | \(V_{CC} = 3.6\) \(V\), \(V_{O} = 0.5\) \(V\) | \(\pm 100\) | \(\pm 100\) | \(\mu\)A |
| **I\(\text{OZPU}^{\S}\)** | \(V_{CC} = 0\) to 1.5 \(V\), \(V_{O} = 0.5\) \(V\) to 3 \(V\), \(\text{TOE} = 0\) | \(\pm 100\) | \(\pm 100\) | \(\mu\)A |
| **I\(\text{OZPD}^{\S}\)** | \(V_{CC} = 1.5\) \(V\) to 0, \(V_{O} = 0.5\) \(V\) to 3 \(V\), \(\text{TOE} = 0\) | \(\pm 100\) | \(\pm 100\) | \(\mu\)A |

\(\dagger\) All typical values are at \(V_{CC} = 3.3\) \(V\), \(T_{A} = 25^\circ C\).

\(\ddagger\) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

\(^{\S}\) This parameter is characterized but not tested.
### Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted) (Continued)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SN54LVT8980</th>
<th>SN74LVT8980</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{CC})</td>
<td>Outputs high (V_{CC} = 3.6, \text{V}, , I_{O} = 0, , V_{I} = V_{CC}) or GND</td>
<td>0.5</td>
<td>0.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Outputs low</td>
<td>7</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Outputs disabled</td>
<td>0.5</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>(\Delta I_{CC})</td>
<td>(V_{CC} = 3, \text{V} \text{ to } 3.6, \text{V},) One input at (V_{CC} - 0.6, \text{V},) Other inputs at (V_{CC}) or GND</td>
<td>0.2</td>
<td>0.2</td>
<td>mA</td>
</tr>
<tr>
<td>(C_{i})</td>
<td>(V_{I} = 3, \text{V}) or 0</td>
<td>4</td>
<td>4</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{io})</td>
<td>(V_{O} = 3, \text{V}) or 0</td>
<td>5</td>
<td>5</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{o})</td>
<td>(V_{O} = 3, \text{V}) or 0</td>
<td>7</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>

† All typical values are at \(V_{CC} = 3.3\, \text{V},\) \(T_{A} = 25^\circ\text{C}\).

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than \(V_{CC}\) or GND.

### Timing Requirements Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted) (See Figures 9 and 10)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>SN54LVT8980</th>
<th>SN74LVT8980</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(f_{clock})</td>
<td>(T_{CK} = \text{CLKIN (CDIV } = 0)</td>
<td>0</td>
<td>20</td>
<td>(0)</td>
</tr>
<tr>
<td></td>
<td>(T_{CK} = \text{CLKIN/2 (CDIV } = 1)</td>
<td>0</td>
<td>40</td>
<td>(0)</td>
</tr>
<tr>
<td></td>
<td>(T_{CK} \leq \text{CLKIN/4 (CDIV } \geq 2)</td>
<td>0</td>
<td>70</td>
<td>(0)</td>
</tr>
<tr>
<td>(t_w)</td>
<td>(\text{CLKIN high or low})</td>
<td>25</td>
<td>31</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td>(T_{CK} = \text{CLKIN (CDIV } = 0)</td>
<td>12.5</td>
<td>15.6</td>
<td>12.5</td>
</tr>
<tr>
<td></td>
<td>(T_{CK} = \text{CLKIN/2 (CDIV } = 1)</td>
<td>7.1</td>
<td>7.8</td>
<td>7.1</td>
</tr>
<tr>
<td></td>
<td>(T_{CK} \leq \text{CLKIN/4 (CDIV } \geq 2)</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>(t_{su})</td>
<td>(A) before (\text{STRB}) (\downarrow) (\text{Read or write (R/W high or low)})</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>(D) before (\text{STRB}) (\uparrow) (\text{Write (R/W low)})</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>(\text{R/W before STRB}) (\downarrow)</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>(\text{TDI before CLKIN}) (\uparrow)</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>(t_h)</td>
<td>(\text{A after STRB}) (\uparrow) (\text{Read or write (R/W high or low)})</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>(D) after (\text{STRB}) (\uparrow) (\text{Write (R/W low)})</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>(\text{R/W after STRB}) (\uparrow)</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>(\text{TDI after CLKIN}) (\uparrow)</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

†† This is the increase in supply current for each input that is at the specified TTL voltage level rather than \(V_{CC}\) or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 9 and 10)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$V_{CC} = 3.3 , V \pm 0.3 , V$</th>
<th>$V_{CC} = 2.7 , V$</th>
<th>$V_{CC} = 3.3 , V \pm 0.3 , V$</th>
<th>$V_{CC} = 2.7 , V$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>CLKIN</td>
<td>TCK</td>
<td>6 20 25</td>
<td>6 10 17 20</td>
<td>6 10 17 20</td>
<td>6 10 17 20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>CLKIN</td>
<td>TDO, TMS</td>
<td>8 35 40</td>
<td>8 18 30 35</td>
<td>8 18 30 35</td>
<td>8 18 30 35</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>RST↓</td>
<td>D</td>
<td>3 35 40</td>
<td>3 17 30 35</td>
<td>3 17 30 35</td>
<td>3 17 30 35</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>RST↓</td>
<td>RDY</td>
<td>3 35 40</td>
<td>3 17 30 35</td>
<td>3 17 30 35</td>
<td>3 17 30 35</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>RST↓</td>
<td>TDO, TMS, TRST</td>
<td>5 30 35</td>
<td>5 15 25 30</td>
<td>5 15 25 30</td>
<td>5 15 25 30</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>TCK</td>
<td>5 30 35</td>
<td>5 15 25 30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>STRB↑</td>
<td>TCK, D, TDO, TMS, TRST discrete mode</td>
<td>3 28 35</td>
<td>3 14 22 28</td>
<td>3 14 22 28</td>
<td>3 14 22 28</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZL}$</td>
<td>STRB↓</td>
<td>TCK, D, TDO, TMS, TRST other modes</td>
<td>6 40 45</td>
<td>6 20 35 40</td>
<td>6 20 35 40</td>
<td>6 20 35 40</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>STRB↑</td>
<td>D</td>
<td>3 20 25</td>
<td>3 8 15 18</td>
<td>3 8 15 18</td>
<td>3 8 15 18</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZL}$</td>
<td>STRB↓</td>
<td>TCK, D, TDO, TMS, TRST</td>
<td>5 30 35</td>
<td>5 15 25 30</td>
<td>5 15 25 30</td>
<td>5 15 25 30</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>TOE↓</td>
<td>TCK, D, TDO, TMS, TRST</td>
<td>2 15 18</td>
<td>2 6 12 15</td>
<td>2 6 12 15</td>
<td>2 6 12 15</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>STRB↑</td>
<td>D</td>
<td>3 20 25</td>
<td>3 8 15 18</td>
<td>3 8 15 18</td>
<td>3 8 15 18</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHZ}$</td>
<td>STRB↑</td>
<td>TCK, D, TDO, TMS, TRST</td>
<td>5 30 35</td>
<td>5 15 25 30</td>
<td>5 15 25 30</td>
<td>5 15 25 30</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>TOE↑</td>
<td>TCK, D, TDO, TMS, TRST</td>
<td>2 15 18</td>
<td>2 6 12 15</td>
<td>2 6 12 15</td>
<td>2 6 12 15</td>
<td>ns</td>
</tr>
</tbody>
</table>

† All typical values are at $V_{CC} = 3.3 \, V$, $T_A = 25^\circ C$. 

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.
PARAMETER MEASUREMENT INFORMATION

NOTE:
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 9. Load Circuit and Voltage Waveforms (D and RDY Outputs)
PARAMETER MEASUREMENT INFORMATION

**LOAD CIRCUIT**

From Output Under Test

\[ C_L = 50 \text{ pF} \]

(see Note A)

500 \( \Omega \)

S1

6 V

○ Open

500 \( \Omega \)

GND

**VOLTAGE WAVEFORMS**

**PULSE DURATION**

Input

1.5 V

1.5 V

0 V

Timing Input

1.5 V

2.7 V

0 V

Data Input

1.5 V

1.5 V

0 V

**VOLTAGE WAVEFORMS**

**SETUP AND HOLD TIMES**

Output Control

1.5 V

1.5 V

0 V

Output Waveform 1

S1 at 6 V

(see Note B)

1.5 V

Output Waveform 2

S1 at GND

(see Note B)

1.5 V

**VOLTAGE WAVEFORMS**

**ENABLE AND DISABLE TIMES**

Low- and High-Level Enabling

Output

1.5 V

1.5 V

0 V

Output

1.5 V

1.5 V

0 V

NOTES:

E. \( C_L \) includes probe and jig capacitance.

F. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

G. All input pulses are supplied by generators having the following characteristics: \( \text{PRR} \leq 10 \text{ MHz}, \ Z_O = 50 \Omega, \ t_r \leq 2.5 \text{ ns}, \ t_f \leq 2.5 \text{ ns} \).

H. The outputs are measured one at a time with one transition per measurement.

**Figure 10. Load Circuit and Voltage Waveforms (TCK, TDO, TMS, TRST Outputs)**
silicon errata

The descriptions and specifications included in this data sheet represent the intended performance of the 'LVT8990 device. In most cases, these descriptions and specifications also represent the actual performance of silicon of a given revision. Specific exceptions are noted here.

item 1 – operation of host interface (STRB) asynchronous to CLKin

The host interface, which is timed by STRB, is intended to be, and properly should be, fully asynchronous relative to CLKin. In short, the device should function as described in this data sheet regardless of the timing relationship between applied STRB and CLKin.

The 'LVT8990 “X” die, however, fails to function properly when STRB is not synchronous to CLKin. Specifically, STRB must be applied considering adequate setup time requirements as follows:

<table>
<thead>
<tr>
<th>UNIT</th>
<th>MIN</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>tsu</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A fix is proposed for device revision 'LVT8980A.

workaround

For an 'LVT8980 “X” die design, always operate the host interface (specifically, STRB) synchronously to CLKin, maintaining setup time requirements as given above. In most applications, this would mean that the eTBDC CLKin is driven from the same original clock source as the host CPU.

item 1 – read of TDI buffer while it is empty (not ready)

When a read is made to TDI buffer while it is empty (not ready), the RDY pin signal is specified to go low, indicating that the eTBC is not presently ready to service the requested access. If, while STRB is held low, subsequent processing of a scan command fills a byte in the TDI buffer, the RDY pin signal is specified to return high, indicating that the eTBC is ready to complete the access. Correspondingly, the available byte of data from TDI buffer should be latched onto the data bus such that the host can access this data.

The 'LVT8990 “X” die, however, does not function properly with respect to the actual data latched to the data bus. That is, if a read is made to TDI buffer while it is empty (not ready), the RDY pin signal goes low as specified; as well, if the STRB pin signal is held low, and further processing of a scan command fills a byte in the TDI buffer, the RDY pin signal returns high as specified. However, at the same time that RDY returns high, the TDI data byte should be latched onto the data bus. If this does not occur, the data that does appear on the data bus is not valid.

A fix is proposed for device revision 'LVT8980A.

workaround

For an LVT8990 “X” design, always poll the TDI buffer (read status register, bit 7, TDIS) to ensure that it is ready prior to a desired read to TDI buffer. Of course, such a software-polled mode versus the hardware-inserted wait-states (RDY) mode (as originally specified, and as proposed to be fixed in 'LVT8980A device revision) places more overhead on the CPU and likely reduces throughput as well.
considerations for migrating 'LVT8990 “X” die designs to 'LVT8980A

As noted above, device revision 'LVT8980A proposes to fix the two known silicon errata of 'LVT8980. It is recommended that designs based on the 'LVT8980 “X” die consider and plan for migration to 'LVT8980A.

In the case of all known silicon errata items, the 'LVT8980A device function will be a super set of the actual function of 'LVT8980 “X” die and will comply with the device descriptions and specifications of this data sheet. So, with respect to the proposed fixes, 'LVT8980JA can directly replace 'LVT8980 “X” die in existing designs.

However, the 'LVT8980A device revision proposes to make an additional change that does not comply with the device descriptions and specifications of this data sheet. This additional change is noted here.

item 1 – make TOE pin signal high enabling and rename to TOFF

The 'LVT8980A device revision proposes to modify the polarity of the TOE (active-low test output enable) pin signal (pin 13 for DW, JT packages) to high enabling and consequently to rename the pin signal to active-low test off (TOFF).

workaround

For an 'LVT8980 “X” die design, it is recommended that the TOE pin be tied off to ground via a discrete resistor. Then, to migrate to use of 'LVT8980A device, the design need only be modified to omit the resistor – the internal resistor at the 'LVT8980A TOFF pin will ensure that it is driven by default to the state required to enable the device TAP outputs.
IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (“CRITICAL APPLICATIONS”). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER’S RISK.

In order to minimize risks associated with the customer’s applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI’s publication of information regarding any third party’s products or services does not constitute TI’s approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated