HUGIN registers (Base address 0x1000)

Address	Bits	Register	Read/Write	Explanation	Remark	Default
000		*UPDATE*	RO	Reading updates all counters		
004		RST_CNT		Reset counters		0
008	0	R_THROUT_ENB		Enable throttle outputs (L0 & L1)		0
020	0	S_EXT_FIFO_EF	RO	Throttle history FIFO empty		
	1	S_EXT_FIFO_PAE	RO	Throttle history FIFO almost empty		
	2	S_EXT_FIFO_HF	RO	Throttle history FIFO half full		
	3	S_EXT_FIFO_PAF	RO	Throttle history FIFO almost full		
	4	S_EXT_FIFO_FF	RO	Throttle history FIFO full		
02C	31 .. 0	RST_SEL_CNT		Reset selected counters	One bit per counter	0
030	15 .. 0	C_L0_THROTTLE0	RO	Total L0 throttle time, input 0		
..	15 .. 0	C_L0_THROTTLEn	RO	Total L0 throttle time, input n		
06C	15 .. 0	C_L0_THROTTLE15	RO	Total L0 throttle time, input 15		
070	15 .. 0	C_L1_THROTTLE0	RO	Total L1 throttle time, input 0		
..	15 .. 0	C_L1_THROTTLEn	RO	Total L1 throttle time, input n		
0AC	15 .. 0	C_L1_THROTTLE15	RO	Total L1 throttle time, input 15		
0C0	31 .. 0	R_FIFO_WRITE_DATA		FIFO write data (Debug)		
0C4	31 .. 0	R_FIFO_READ_DATA		FIFO read data (Debug)		
0F8	15 .. 0	TEST		Local bus test register		0
0FC	15 .. 0	VERSION	RO	Version number of the VHDL code	Date in decimal YEAR|MO|DA|HR	