ODIN Q_L0 registers (Base address 0x2000)

Version: 2.3 **2006.06.28**

Address	Bits	Register	Read/Write	Explanation	Remark	Default
000	0	R_L0_THR		L0 throttle from ECS	Pause, does not stop trigger counters	0
004	0	R_L0_EXT_ENB		Enable external L0 trigger input		0
	1	R_L0_SNCCHK_ENB		Enable L0 synchronization check	Reject L0 synch errors	0
	2	R_L0_SNCERR_KEEP		Keep L0 synchronization errors	Keep both accepts and rejects	0
	3	R_AUXTRG_ENB		Enable auxillary L0 triggers		0
	4	R_AUXTRG_FRC		Force all auxillary L0 triggers		0
	5	R_PERTRG_A_ENB		Enable periodic L0 trigger A		0
	6	R_PERTRG_B_ENB		Enable periodic L0 trigger B		0
	7	R_RNDGEN_ENB		Enable random generator	Loads the random seeds on enable	0
	8	R_RNDTRG_A_ENB		Enable random L0 trigger A		0
	9	R_RNDTRG_B_ENB		Force all random L0 triggers B		0
	10	R_SEQTRG_ENB		Enable trigger sequence	pattern of up to 3564 L0 triggers	0
	11	R_TIMTRG_ENB		Enable timing L0 trigger		0
	12	R_L0_MAX_ENB		Enable limited number of L0 triggers	Stops after R_L0_MAX triggers	0
	13	R_BXSEQ_ENB		Enable bunch crossing type sequencer		0
	14					
	15					
008	0	R_EXT1_L0THR_ENB		Enable external L0 throttle, connector 1		0
	1	R_EXT2_L0THR_ENB		Enable external L0 throttle, connector 2	Version V1 only	0
	2	R_L0EMU_L0THR_ENB		Enable L0 throttle from L0 derandomizer emulator	This you could play with to see the emulator in action	0
	3	R_FIFO_L0THR_ENB		Enable L0 throttle from FIFOs (AFIFO and FEB)		0
	7 .. 4	P_L0_GAP_LEN		L0 gap length		0
00C	0	DMND_PERTRG_A	WO	Demand a single L0 trigger A	Sent at the crossing defined by the offset	
	1	DMND_PERTRG_B	WO	Demand a single L0 trigger B	Sent at the crossing defined by the offset	
010	0	RST_PERTRG_A		Reset periodic L0 trigger A		0
	1	RST_PERTRG_B		Reset periodic L0 trigger B		0
	2	RST_L0EMU		Reset L0 derandomizer emulator		0
	3	RST_SEQTRG		Reset trigger sequencer		0
	4	RST_BXSEQ		Reset bunch crossing sequencer		0
014	7 .. 0	P_L0_LATENCY		L0 trigger latency in ODIN	Applies to L0 trigger input and auxillary trigger input	0
	15 .. 8	P_BX_INFO_LATENCY		Latency of data on BX information input		0
	19 .. 16	P_BCR_DEL		Delay of BCR/ECR for local BID/EID counters		0
	20	H_L0_PHASE		Sampling edge of external L0 trigger	0 = rising edge of clock	0

018	15 .. 0	P_L0_MAX		Maximum number of L0 triggers in limited run		0
	18 .. 16	P_TIMTRG_WIN		Length of timing trigger window	window = timing trigger +/- P_TIMTRG_WIN	0
	19		unused			
	23 .. 20	P_AUXTRG_NTRG		Number of auxillary L0 triggers in burst		0
	24	P_AUXTRG_EDGE_ENB		Enable triggering on edge on auxillary input	Otherwise level triggered	0
01C	4 .. 0	P_L0D_LOCCUPANCY		L0 derandomizer lower occupancy	For instance…	12
	7 .. 5		unused			
	12 .. 8	P_L0D_UOCCUPANCY		L0 derandomizer upper occupancy		14
	15 .. 13		unused			
	21 .. 16	P_L0D_RO_TIME		L0 derandomizer readout time	value + 1	10
020	23 .. 0	P_PERTRG_A_PER		Periodicity of periodic L0 trigger A	value + 1	0
024	11 .. 0	P_PERTRG_A_OFS		Offset of periodic L0 trigger A		0
	16 .. 12	P_PERTRG_A_NTRG		Number of L0 trigger A accepts in burst		0
028	23 .. 0	P_PERTRG_B_PER		Periodicity of periodic L0 trigger B		0
02C	11 .. 0	P_PERTRG_B_OFS		Offset of periodic L0 trigger B		0
	16 .. 12	P_PERTRG_B_NTRG		Number of L0 trigger B accepts in burst		0
030	31 .. 0	P_RNDGEN_SEED_A		Random generator seed A		0
034	31 .. 0	P_RNDGEN_SEED_B		L1 random generator seed B		0
038	31 .. 0	P_RNDGEN_THRESH_A		Random generator threshold A	frequency_L0 = P_L0_THRESH / (2**32-1) * 40 MHz	0
03C	31 .. 0	P_RNDGEN_THRESH_B		Random generator threshold B	Not used currently	0
040	31 .. 0		unused			
044	0	S_EXT1_L0THR	RO	External L0 throttle status, connector 1		
	1	S_EXT2_L0THR	RO	External L0 throttle status, connector 2	Version V1 only	
	2	S_L0EMU_L0THR	RO	L0 throttle from L0 derandomizer enulator		
	3	S_L0_INH	RO	Status of global L0 inhibit (throttles etc)		
	4	S_L0_GAP	RO	Status of L0 gap generator		
	5	S_AFIFO_FULL_CONT	RO	AFIFO full continuous status		
	6	S_AFIFO_FULL_INST	RO	AFIFO got full instantaneously	Reset by counter reset	
	7	S_L0_AUTO_STOP	RO	L0 auto stop from maximum L0 trigger run		
	8	S_SNCERR_INST	RO	L0 synchronization error instantaneously		
	9	S_SNCERR_CONT	RO	L0 synchronization error continuous		
	10	S_FEB_FULL_CONT	RO	FEB full continuous status		
	11	S_FEB_FULL_INST	RO	FEB got full instantaneously	Reset by counter reset	
048	11 .. 0	C_BID_INT	RO	Bunch ID from ODIN internal counter		
	23 .. 12	C_BID_EXT	RO	Bunch ID as received from L0DU		
	28 .. 24	C_L0D_OCCUPANCY	RO	L0 derandomizer occupancy from emulator		
04C	7 .. 0	INT_BXSEQ_ADDR		Address for writing to bunch crossing sequence memories	bit 7 determines memory for beam 1(=0) or 2(=1)	0

050	31 .. 0	INT_BXSEQ_DATA		Data to be written to bunch crossing sequence memory		0
054	31 .. 0	RST_SEL_CNT		Reset selected counters	One bit per counter	0
058	23 .. 0	C_SNCERR	RO	Number of synch errors		
05C	23 .. 0	C_SNCERR_REJ_TOT	RO	Total number of synch errors rejected		
060	23 .. 0	C_SNCERR_REJ_GT	RO	Gated number of synch errors rejected		
064	31 .. 0	C_L0ACC_EXT	RO	Total number of external L0 accepts (incoming)	Number of L0 accepts from L0DU	
068	31 .. 0	C_L0ACC_EXT_TOT	RO	Total number of external L0 accepts	Number of external L0 accepts after priority scheme	
06C	31 .. 0	C_L0ACC_EXT_GT	RO	Gated number of external L0 accepts		
070	23 .. 0	C_PERTRG_A_TOT	RO	Total number of periodic L0 triggers A		
074	23 .. 0	C_PERTRG_A_GT	RO	Gated number of periodic L0 triggers A		
078	23 .. 0	C_PERTRG_B_TOT	RO	Total number of periodic L0 triggers B		
07C	23 .. 0	C_PERTRG_B_GT	RO	Gated number of periodic L0 triggers B		
080	23 .. 0	C_CALTRG_A_TOT	RO	Total number of calibration L0 triggers A		
084	23 .. 0	C_CALTRG_A_GT	RO	Gated number of calibration L0 triggers A		
088	23 .. 0	C_CALTRG_B_TOT	RO	Total number of calibration L0 triggers B		
08C	23 .. 0	C_CALTRG_B_GT	RO	Gated number of calibration L0 triggers A		
090	23 .. 0	C_CALTRG_C_TOT	RO	Total number of calibration L0 triggers C		
094	23 .. 0	C_CALTRG_C_GT	RO	Gated number of calibration L0 triggers A		
098	31 .. 0	C_AUXTRG_TOT	RO	Total number of auxillary L0 triggers		
09C	31 .. 0	C_AUXTRG_GT	RO	Gated number of auxillary L0 triggers		
0A0	15 .. 0	C_TIMTRG_TOT	RO	Total number of timing L0 triggers		
0A4	15 .. 0	C_TIMTRG_GT	RO	Gated number of timing L0 triggers		
0A8	31 .. 0	C_RNDTRG_TOT	RO	Total number of random L0 triggers		
0AC	31 .. 0	C_RNDTRG_GT	RO	Gated number of random L0 triggers		
0B0	31 .. 0	C_ORBIT	RO	Number of LHC turns		
0B4	31 .. 0	C_L0ACC_TOT1	RO	Total number of L0 trigger accepts		
0B8	61 .. 32	C_L0ACC_TOT2	RO			
0BC	31 .. 0	C_L0ACC_GT1	RO	Gated number of L0 trigger accepts		
0C0	61 .. 32	C_L0ACC_GT2	RO			
0C4	23 .. 0	C_L0FRC_EXT	RO	Number of forced external L0 triggers		
0C8	23 .. 0	C_L0FRC_TOT	RO	Total numberf of forced L0 triggers		
0CC	23 .. 0	C_L0FRC_GT	RO	Gated number of forced L0 triggers		
0D0	23 .. 0	C_L0THR_EXT	RO	Total time of external L0 throttle	Number of bunch clocks	
0D4	31 .. 0	C_L0INH_TOT	RO	Total time of global L0 inhibit	Number of bunch clocks	
0D8	6 .. 0	INT_SEQTRG_ADDR		Address for writing to trigger sequencer memory		0
0DC	31 .. 0	INT_SEQTRG_DATA		Data to be written to trigger sequencer memory		0
0E0	-	*TST_FIFO_WE*	WO	Write test data to FEB and AFIFO	Dataless, only if Q_L0 set in test mode (TST_MODE = 1)	

0E4	31 .. 0	TST_FIFO1_OUT		Test data for testing FEB and AFIFO		0
0E8	31 .. 0	TST_FIFO2_OUT		Test data for testing FEB and AFIFO		0
0EC	15 .. 0	TST_L0LINK	RO	Current value on L0 trigger input, L0 link test	Sampled by update counters	
	31 .. 16	TST_L0LINK_CNT	RO	Current value on internal test counter, L0 link test	Sampled by update counters	
0F0	11 .. 0	L0_BID	RO	Current state of L0_BID lines on L0 trigger input		
	12	L0_DECISION	RO	Current state of L0 decision line on L0 trigger input		
	13	L0_FORCE	RO	Current state of L0 force line on L0 trigger input		
	14	L0_TIM_TRG	RO	Current state of L0 timing trigger line on L0 trigger input		
	15	L0_RESERVE	RO	Current state of L0 reserve line on L0 trigger input		
	23 .. 16	BX_DATA	RO	Current state of BX data input		
	24	L0_THR_EXT1	RO	Current state of L0 throttle line on throttle input 1		
	25	L0_THR_EXT2	RO	Current state of L0 throttle line on throttle input 2		
	26	AUX_TRG	RO	Current state of auxillary trigger input		
0F4	0	TST_MODE		Set Q_L0 in test mode		0
	1	TST_L0LINK_ENB		Set L0 trigger input in counter test mode	Test counter starts on 0xFFFF on input	0
0F8	31 .. 0	TST_LBUS		Local bus test register		0
0FC	31 .. 0	VERSION	RO	Version number of the VHDL code	Date in decimal YEAR|MO|DA|HR	