THOR registers (Base address 0x1000)

Address	Bits	Register	Read/Write	Explanation	Remark	Default
000	3 .. 0	SELECTION0		Input selection for output 0		0
004	3 .. 0	SELECTION1		Input selection for output 1		0
008	3 .. 0	SELECTION2		Input selection for output 2		0
00C	3 .. 0	SELECTION3		Input selection for output 3		0
010	3 .. 0	SELECTION4		Input selection for output 4		0
014	3 .. 0	SELECTION5		Input selection for output 5		0
018	3 .. 0	SELECTION6		Input selection for output 6		0
01C	3 .. 0	SELECTION7		Input selection for output 7		0
020	3 .. 0	SELECTION8		Input selection for output 8		0
024	3 .. 0	SELECTION9		Input selection for output 9		0
028	3 .. 0	SELECTION10		Input selection for output 10		0
02C	3 .. 0	SELECTION11		Input selection for output 11		0
030	3 .. 0	SELECTION12		Input selection for output 12		0
034	3 .. 0	SELECTION13		Input selection for output 13		0
038	3 .. 0	SELECTION14		Input selection for output 14		0
03C	3 .. 0	SELECTION15		Input selection for output 15		0
040	6 .. 0	DELAY0		Delay value for output 0		0
044	6 .. 0	DELAY1		Delay value for output 1		0
048	6 .. 0	DELAY2		Delay value for output 2		0
04C	6 .. 0	DELAY3		Delay value for output 3		0
050	6 .. 0	DELAY4		Delay value for output 4		0
054	6 .. 0	DELAY5		Delay value for output 5		0
058	6 .. 0	DELAY6		Delay value for output 6		0
05C	6 .. 0	DELAY7		Delay value for output 7		0
060	6 .. 0	DELAY8		Delay value for output 8		0
064	6 .. 0	DELAY9		Delay value for output 9		0
068	6 .. 0	DELAY10		Delay value for output 10		0
06C	6 .. 0	DELAY11		Delay value for output 11		0
070	6 .. 0	DELAY12		Delay value for output 12		0
074	6 .. 0	DELAY13		Delay value for output 13		0
078	6 .. 0	DELAY14		Delay value for output 14		0
07C	6 .. 0	DELAY15		Delay value for output 15		0
080	15 .. 0	ENABLE		Output enables for output 0 - 15	Output enabled by bit set	0

084		*RESET*	WO	Reset of all registers	Data less	
0F8	15 .. 0	TEST		Local bus test register		0
0FC	15 .. 0	VERSION	RO	Version number of the VHDL code	Date in decimal YEAR|MO|DA|HR	