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“How can I run my detector?”

Readout Partitioning and Running Modes

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ABSTRACT

The LHCb experiment will go through phases of commissioning, testing, calibrations, debugging, and data taking. A lot of effort has been put into identifying the modes of running, the functionality, and the system design required to efficiently accomplish these tasks. This document will hopefully serve as an introductory guide to utilising the system by describing it from a point of view of usage and by outlining a number of running scenarios.

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1 Introduction

Testing the sub-detector Front-End electronics will soon be an integral part of everyday life in LHCb, and soon enough we will be faced with the task of commissioning, and later, routinely carry out calibrations, physics data-taking, testing, and debugging. These different operations require a wide spectrum of functionality and running modes.

The TFC system[1] is designed with the endeavour to provide a versatile system that can support these different stages and types of detector operations without modifications. In order to aid people involved in the design of the detectors, the design of the Front-End electronics, and testing, this document aim at giving an overview of the system from a user point of view. It focuses entirely on using the system with the purpose of exercising the Front-End electronics and the readout of data. It does not describe how to commission and test detector control components.

In order to be concrete, the functionality of the system and the partitioning concept are described in the context of different running scenarios:

- Testing a detector "at home" before the LHCb TFC components are available.
- Testing a detector "at home" when the LHCb TFC components are available.
- TTC fibre tests of a detector in situ.
- Commissioning/testing/debugging a detector stand-alone in situ.
- Time alignment of a detector.
- Calibrating a detector.
- Physics data-taking.

At the end, there is also a summary of the user parameters that determines the functionality and a summary of some of the monitoring information that the system provides. In this respect, the document can aid designing the user interface that will eventually be used to control the system.

The document does not describe automated TFC functionality, which is implemented to ensure the correct running of the system, such as counter resets, synchronisation checks, electronics resets, error handling etc.

The document attempts at being short and concise in order to encourage reading. Note that it does not replace any of the detailed documentation referenced in Section 8 and does not describe all the features that the design of the Front-End electronics has to take into account.

2 TFC System Architecture

The Timing and Fast Control (TFC) system controls the distribution of timing, trigger, and control information to the Front-End electronics. In order for this information to arrive synchronously, the TFC system provides means to achieve timing alignment at the Front-End electronics. The system incorporates functionality to prevent buffer overflows in the entire readout chain, and provides means of different types of auto-triggering for tests and calibrations. The TFC system also supports readout partitioning in order to be able to run small sub-systems independently in special running modes. In addition, it provides statistics on the performance of the synchronous readout.

More specifically the information distributed includes the following:

- LHC reference clock at ~40 MHz as received from the LHC timing generators via the LHC machine interface (TTCmi). This clock drives all the electronics in the synchronous readout.
- L0 and L1 trigger decisions.
- Commands resetting event related counters in the Front-End electronics used to identify the accepted events and to check synchronisation.
- Commands resetting the Front-End electronics in order to prepare them for data taking or to recover from an error condition.
- Calibration commands activating a specific calibration system in the Front-End electronics or in the detector. The TFC system has a mechanism to guarantee that the triggers corresponding to the calibration events are accepted.

The TFC architecture is shown in Figure 1. The TFC master is the Readout Supervisor ("Odin"[1])[2]. It receives the LHC bunch clock and the orbit signal from the LHC machine interface (TTCmi)[3], and the L0 and the L1 triggers from the trigger decision units, and has the crucial task of providing the functionality listed above. For what concerns buffer overflows, they are prevented by monitoring the occupancy of the buffers in two different ways. The occupancy of the L0 de-randomiser and the L1 buffer in the Front-End electronics are emulated centrally by the Readout Supervisor. Buffers further down the readout chain monitor the occupancy locally and, in case the buffers get nearly full, signal the Readout Supervisor via a hardwired signal. Overflow is prevented in the Readout Supervisor by throttling the triggers, i.e. converting trigger accepts to trigger rejects until the occupancy is reduced.

The system architecture incorporates a pool of Readout Supervisors, one of which is used for normal data taking. The other Readout Supervisors are reserves and can be invoked for tests, calibrations and debugging. The reserve Readout Supervisors also allow connecting local trigger units.

The trigger splitters allow connecting the L0 and the L1 trigger decision units to several Readout Supervisors. In this way, physics triggers can be used for stand-alone testing as will be explained in Section 5.5. If the "central" RS would break, it also avoids all manual intervention when swapping for another Readout Supervisor.

[1] Odin is the God of all Gods in the Norse mythology.

The TFC Switch ("Thor"[2])[4] is a programmable patch panel that allows distributing the synchronous information from the different Readout Supervisors to the Front-End electronics of all the sub-detectors and the trigger systems.

The distribution network is based on the RD12 Trigger, Timing, and Control (TTC) system[3] and utilises the TTCtx for the electrical-to-optical conversion. The TTC system conveys the clock, channel A is used to transmit the L0 trigger decisions in the form of a accept/reject signal at 40 MHz, and channel B transmits the following information in the form of short TTC broadcasts:

- Transmission of the commands to reset the Bunch Counter (BCR) and the Event Counter (ECR). The Bunch Counter counts bunch-crossings, and the Event Counter counts the number of accepted L0 triggers, which in LHCb is referred to as the L0 Event ID.
- Transmission of the L1 trigger decision.
- Transmission of Front-End control commands, e.g. electronics resets, calibration pulse triggering etc.

TTC receiver chips (TTCrx) implemented in the Front-End electronics receive the TTC signals, decode the channel A and B, and deserialize the channel B broadcasts. The TTC receiver chip also provides means to adjust the timing of the TTC information in order to time align all Front-End electronics. The clock, the channel A and channel B can be adjusted grossly by 16 steps of one clock cycle and finely by 250 steps of 100 ps.

The L1 trigger decision broadcast contains a 3-bit L1 trigger qualifier[5][2] with the trigger type. It can be decoded by the Front-End electronics and used to invoke special actions.

The Throttle Switch ("Munin"[3])[4] function in the opposite sense of the TFC Switch and feed back external trigger throttle signals to the appropriate Readout Supervisors in case of imminent buffer overflows. The system incorporates two Throttle Switches, a L0 and a L1 Throttle Switch. The sources of the L0 trigger throttles are essentially the components that feed the L1 trigger system. The sources of the L1 trigger throttles are the L1 de-randomisers and components in the data-driven part of the DAQ system.

The Throttle ORs[4] form a logical OR of the throttle signals from sets of Front-End electronics and readout components further down the readout chain.

A GPS system allows time stamping experiment status information that is sampled in the RS.

[2] Thor is the God of Thunder and Odin's son.

[3] Munin is one of Odin's two ravens. They bring Odin news from all over the world.

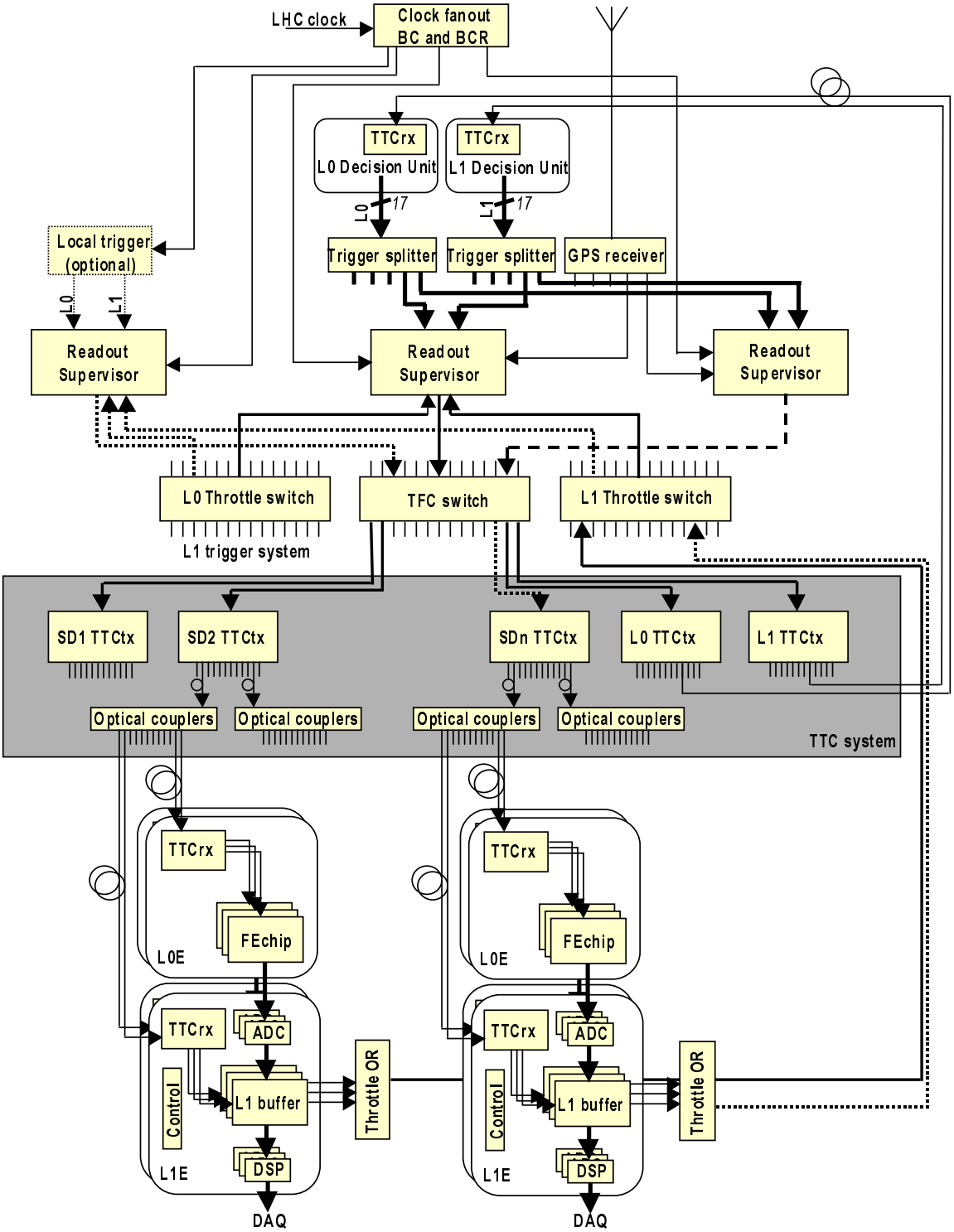


Figure 1: Overview of the TFC architecture.

3 Readout Partitioning

The TFC system has been designed with emphasis on partitioning[6] and allows sets of Front-End electronics to be operated individually. In particular, a *readout (TFC-) partition* is a generic term defining a configurable ensemble of parts of the readout system that can be operated concurrently, independently, and with a different timing, triggering, and control configuration than any other partition. Obviously, the TFC architecture defines a minimal sub-system that can be factorised out. These are so-called *partition elements*, in other words the smallest sub-system that can be operated stand-alone.

Figure 2 is a simplified version of the TFC architecture in Figure 1. The TFC Switch realises the partitioning and allows setting up a partition by associating a number of partition elements to a specific Readout Supervisor. The Readout Supervisor can then be configured via the ECS to control and trigger the partition in whatever specific running mode that is required. From the architecture of the system it follows that the Front-End electronics that is fed by the same output of the TFC Switch is receiving the same timing, trigger, and control information. That is, a part of the Front-End electronics connected to a TFC Switch output can not be operated in different running mode than another part belonging to the same output. Hence, the association of the Front-End electronics to the different outputs of the TFC Switch defines the boundaries between the smallest sub-systems, partition elements, which can be operated independently.

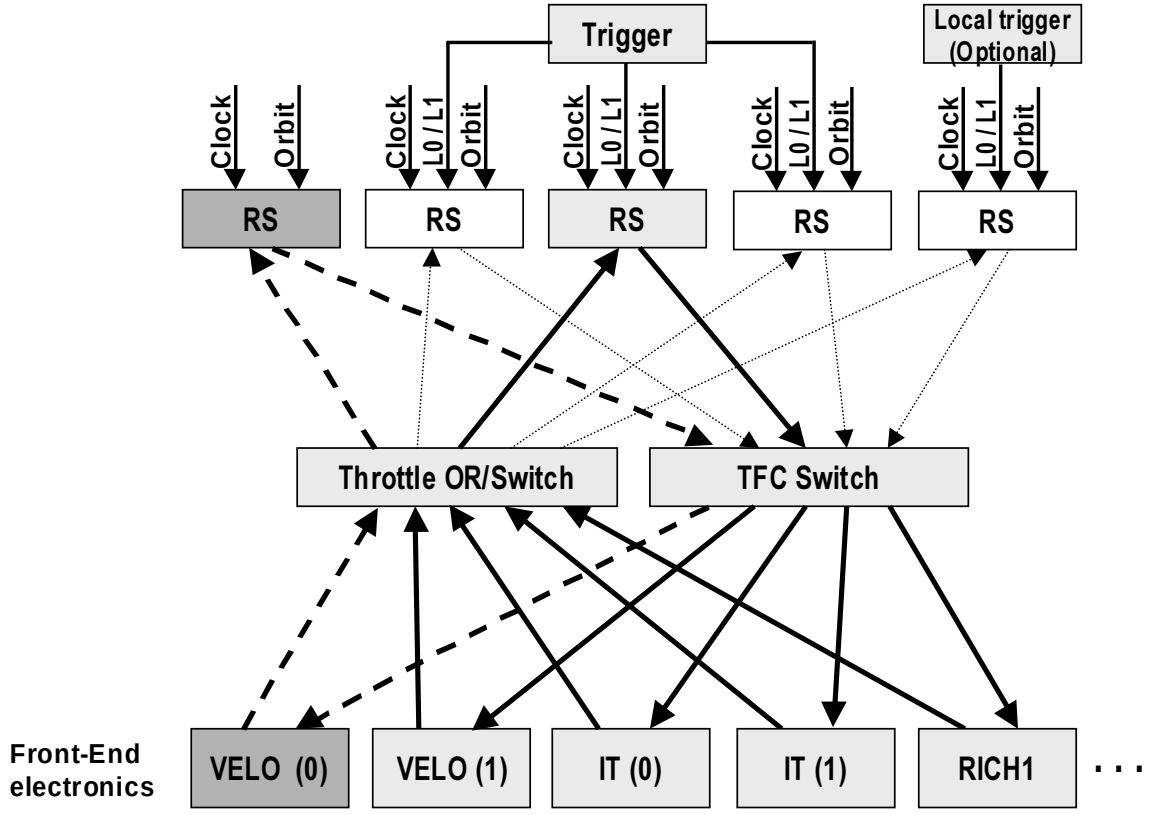


Figure 2: The TFC architecture simplified to show an example of partitioning.

In summary, setting up a functional partition means to reserve a Readout Supervisor to drive the partition and configure the Switches with the appropriate paths to the partition elements in question. In addition, whatever is needed to operate the partition in terms of control system is added automatically using a configuration database

In Figure 2, the "(0)" and "(1)" after the sub-detector name indicate that the sub-detector is divided into two independent partition elements. In this example, the partition elements VELO (1), IT (0), IT (1), RICH1, etc form a partition which is running with the "central RS", receiving triggers from the central triggers. Partition element VELO (0) forms another partition and is simultaneously running a stand-alone run with a separate RS. The three other Readout Supervisors are idle and can be reserved at any time for setting up and driving other partitions.

The TFC Switch has been designed to have 16 inputs and 16 outputs, and therefore allows the LHCb detector to be divided into 16 partition elements. Reserving one output for the L0 trigger partition element and one output for the L1 trigger partition element, the detector Front-End could be divided into 14 partition elements. A possible sub-division of the LHCb detector is presented in Table 1. To increase the partition granularity an option exist whereby four TFC Switches are deployed in order to subdivide the LHCb detector into 32 partitions.

In some cases, the size of a TFC partition element may be inconvenient to efficiently test or debug a problem, since each of the TFC partition elements cover a relatively large amount of Front-End electronics. Another case is if a fraction of a partition element is not functioning properly and has to be excluded. To handle this the concept of masking has been introduced. This mechanism requires support in the Front-End electronics. It has been specified that at minimum masking should be possible at the level of sources to the L1 Front-End electronics[7]. It is important to observe that although masking may mean that several components become idle they cannot be used for other independent tests. They are still associated to the partition element as in any other case.

A special case is during the commissioning of the sub-detectors. It will probably be extremely useful to be able to test very small parts of the Front-End electronics stand-alone (single TTCrx or a few TTCrx's) in a direct way without the TFC Switch and the long network of fibres between the counting room and the Front-End. As explained in Section 12, this is possible using a "portable" TFC test bench.

Table 1: The table presents a possible configuration with the LHCb detector sub-divided into 16 TFC partition elements.

Detector	**16 elements**
VELO	2
IT	2
RICH 1	1
RICH 2	2
OT	2
PRS + SPD	1
ECAL	1
HCAL	1
MUON	2
L0 trigger	1
L1 trigger	1

In addition to the running mode, the purpose of a particular partition dictates how the partition and its resources are configured. Running a readout partition may mean only exercising the Front-End electronics. However, if the purpose is data taking and processing of the data is necessary, the partition must also involve the rest of the DAQ chain and the L2/L3 farm. Specifying the purpose is a part of reserving a partition and a database will hold all information about which components have to be associated and how they have to be configured.

A mechanism of partition ownership will control the usage of the components in order to allow many people to carry out tests at the same time while avoiding conflicts.

4 Configuring the System

Setting up a "ready-to-roll" detector partition and running it is done using the ECS software and involves several things:

- Defining a partition by selecting the partition elements (e.g. VELO(0), VELO(1), IT (0), IT(1) etc) to read out. This will reserve the partition elements and will allow to take control of the different hardware components involved, e.g. Front-End electronics, power supplies, etc
- Specifying its purpose. This will determine which running modes that will be allowed for the partition and which additional resources will be allocated, typically from the TFC system and the DAQ system, and hence also the related control system components.
- Specifying the modes of running, i.e. configure the Readout Supervisor allocated for the partition with the desired functionality.
- Configuring the detector control system, e.g. switching on the power, download software and calibration data to Front-End electronics, etc. This will clearly depend on the purpose of the partition and the running mode.
- Interact with the system to control the running, e.g. start/stop data taking.

The Readout Supervisor, the Switches, and the Front-End electronics, as well as all other components in the online system, will receive all their configuration data via the ECS interfaces located on-board. There is no possibility to configure the Front-End electronics via the TTC system.

All Readout Supervisor functionality described in this document is permanently residing in the FPGAs of the RS. The functionality is configured and activated for different running modes only via parameters that can be written at any time[4].

All the configuring and the control listed above are carried out via context dependent ECS graphical user interfaces (GUI)[8]). They are organised in a hierarchical structure with an increasing level of abstraction and automation, such that the settings of a specific item that can be controlled at one level is taken from a database with pre-defined values when using a higher level of generalised control interface. An example of a run control display is shown in Figure 3. To change a specific parameter related to the data acquisition, one would e.g. open the "DAQ sub-system run control" by clicking on the "DAQ button" etc.

[4] Obviously, there will be protection against writing parameters that may change the running mode etc during operation.

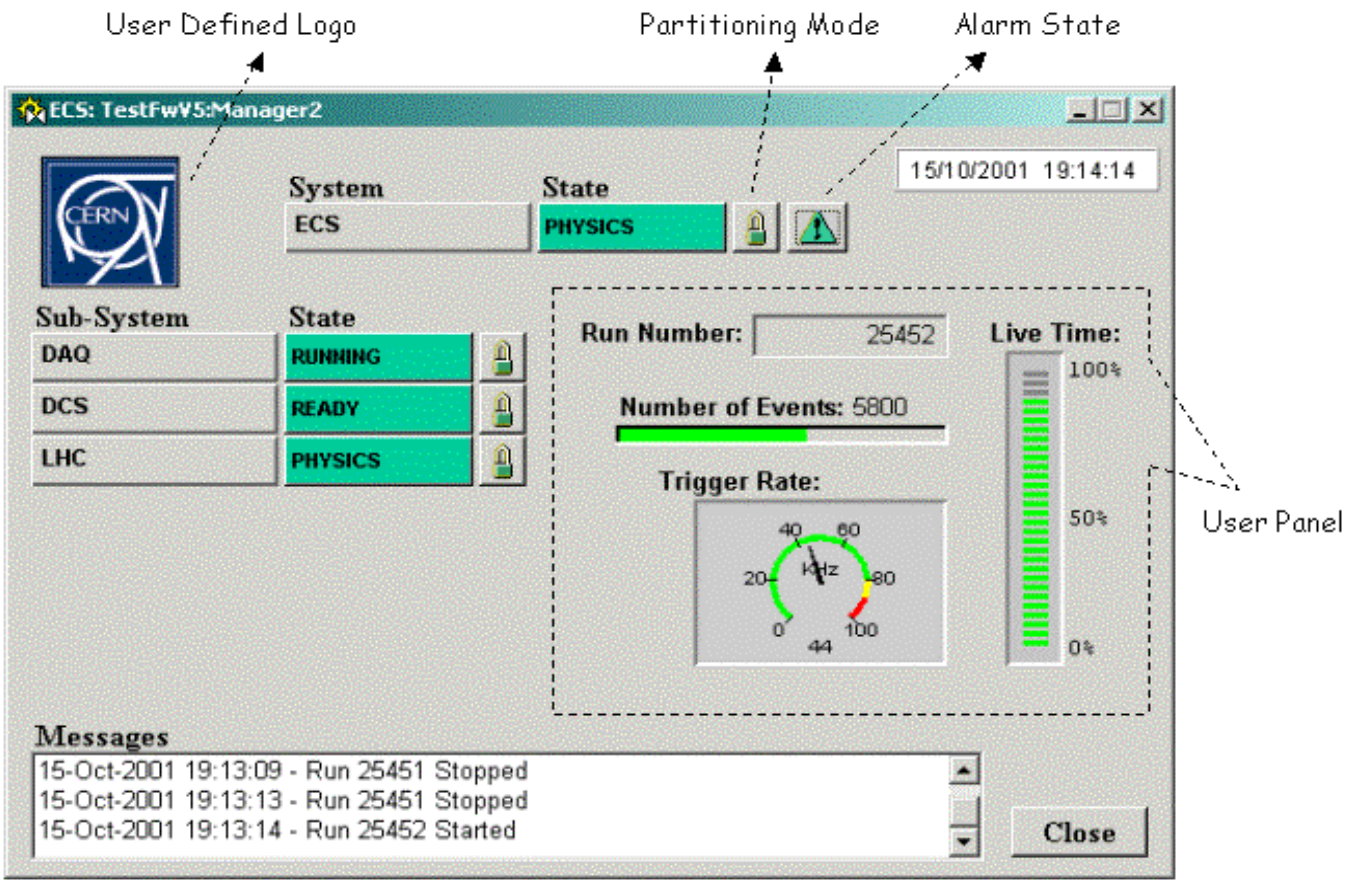


Figure 3: Prototype run control GUI.

5 Running Scenarios

5.1 Testing a detector "at home" before the TFC modules are available

The TFC components specific to LHCb (Readout Supervisor and Switches) are currently (November 2001) in the prototyping phase and will not be available in quantities during 2002. However, Figure 4 shows a simple test bench that has been devised using existing standard TTC equipment that in most cases is sufficient for the initial tests of the Front-End electronics.

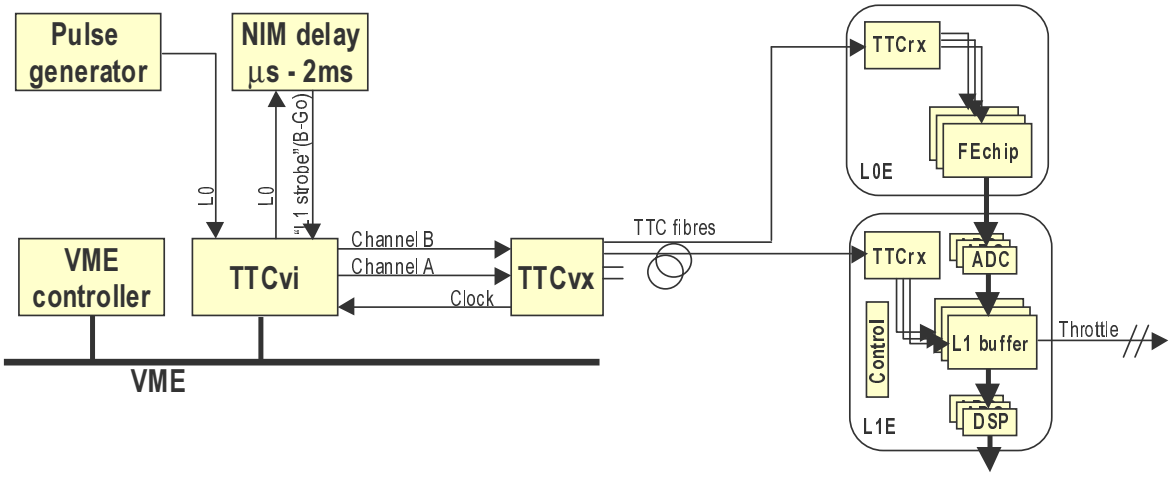


Figure 4 : Test bench setup using general TTC equipment to test the Front-End electronics.

The test bench utilises a TTCvi[9] in a special software configuration to send triggers and channel B broadcasts. Through the VME controller, the test bench allows:

- Sending single L0 triggers.
- Sending single short broadcasts (L1 triggers, electronics resets, and control commands as defined for the TFC system).
- Sending periodic or random L0 triggers (no L1 triggers) at any rate depending on the type of pulse generator that is used. The TTCvi itself has a random generator that allows up to a maximum of 100 kHz.
- Sending periodic or random L0 triggers at a rate up to ~1.7 MHz[5], followed by L1 trigger broadcasts after a fixed latency defined by the NIM delay. The sequence of L1 triggers must be predefined, as they have to be stored in the FIFO on the TTCvi. This allows only a short pattern of L1 triggers as the FIFO is 256 deep, but the FIFO can work in a retransmit mode to enable continuous running.

One limitation using the TTCvi is that there is no way to combine the functionality above with

[5] 1.7 MHz is approximately the maximum rate of short broadcasts that the TTCvi allows.

sending periodically Bunch Counter Resets and Event Counter Resets. If these resets are needed they can be sent together with one of the L1 triggers pre-stored in the TTCvi FIFO. However, depending on how the L0 trigger is set up they may not be sent with an exact period, and in addition the resets will be transmitted every 256th L1 trigger.

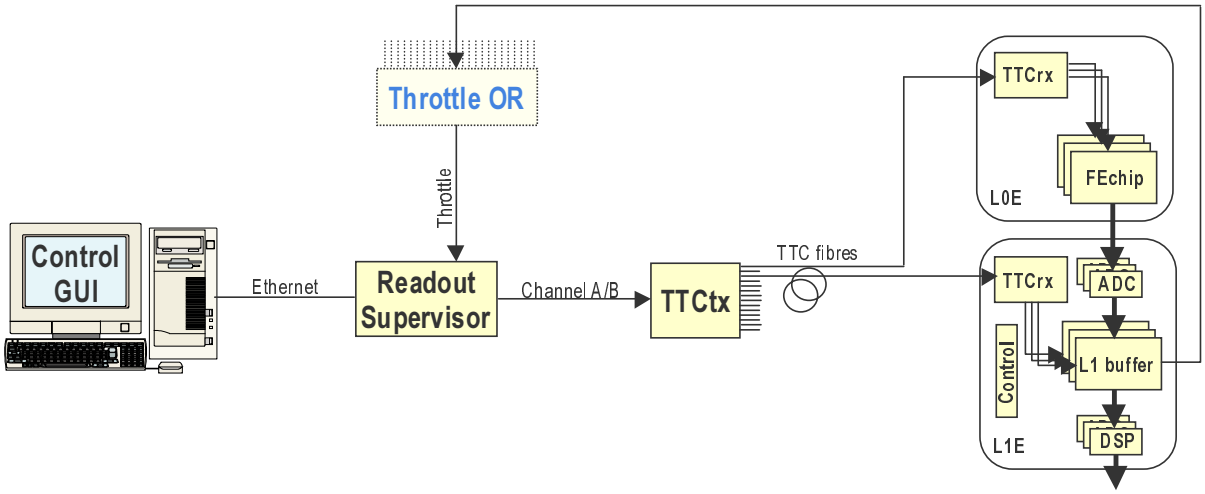
The TTCvx is a TTC encoder with four optical transmitters to drive four TTCrx's. If more destinations are needed, the TTCvx has an electrical output of the encoded TTC signal to drive a TTCtx, which has 14 optical outputs and can drive the TTC optical splitters (32 destinations).

The test bench does not provide for throttle handling, as the L1 decisions pre-stored in the FIFO cannot be modified while running.

5.2 Testing a detector "at home" when the TFC modules are available

Once the Readout Supervisor becomes available the TFC functionality can be fully exploited in any test bench. The Readout Supervisor has an internal 40 MHz clock and an artificial orbit signal in order to emulate authentic running.

A test bench with the Readout Supervisor requires a TTCtx as Figure 5 shows, and optionally an optical coupler if there are more than 14 destinations. A Throttle OR may also be needed to concentrate the throttle signal, as the RS only has one throttle input for each level. The Readout Supervisor only requires one external +5V power supply and forms all other voltages on-board



using DC/DC converters. By connecting a power-supply directly via the on-board IBM-PC type power connector, the Readout Supervisor can be used without a crate. However, a 6U-VME crate is still needed to power the TTCtx.

A special control GUI will be designed to control the Readout Supervisor stand-alone. The repertoire of functions and running modes to test the Front-End electronics are the same as described in Section 5.3, 5.5, and 5.9 below.

5.3 TTC fibre tests of a detector

It may be of interest to make tests of the TTC fibres, and test in a debugging manner how the Front-End electronics respond to the timing, trigger, and fast control signals. A special run option will

exist whereby triggers and any control commands can be fired on a single shot basis.

5.4 Commissioning a sub-detector/FE in situ

During the early commissioning it will probably be necessary to test independently smaller parts of the Front-End electronics than is possible when the partitioning is handled by the TFC Switch and therefore the number of partition elements are limited to 16 (Table 1). To achieve this, it will be possible to run independently Front-End electronics covered by a single TTCrx, or a group of TTCrx's, by using a "portable" test bench consisting of a Readout Supervisor, a TTCtx, and a PC for the control as in Figure 5. Only the number of Readout Supervisors available limits the number of tests that can run in parallel. The repertoire of functions and running modes is described below in Section 5.3, 5.5, and 5.9 below.

Table 1 presents the final partitioning scheme that will be adopted to commission the sub-detectors together and for the running of the experiment. The test bench option will still remain for debugging difficult problems but note that it involves manual intervention then in terms of unplugging the standard TFC fibre and replacing it with the test fibre. Also, one cannot rely on the timing alignment being correct with the test bench.

5.5 Testing/debugging a detector stand-alone in situ

Running a detector stand-alone begins by selecting the partition elements to run via an ECS GUI. This will reserve the partition elements if they are not in use, reserve a Readout Supervisor, and configure the TFC Switch and the Throttle Switches in order for the TFC signals and the throttle signals, respectively, to be passed to the appropriate destinations.

Testing may imply only the Front-End electronics of the detector, but may also include the complete DAQ chain depending on the purpose of the test.

The Readout Supervisor provides a range of triggering possibilities:

- **Random triggers**. The Readout Supervisor can produce random L0 triggers according to a Poisson distribution at a programmable rate between 0.01 Hz and 1.5 MHz[6]. The random L0 triggers can either all be accepted at Level-1, or all be rejected, or be randomly accepted using a second random generator with a programmable rate between η_{L0} */(2**32-1)* and $\eta_{L0,}$ where η_{L0} is the rate of the L0 random trigger. An internal mechanism also emulates the latency of the L1 triggers. Although the latency is fixed it can be programmed.
- **Periodic triggers**. The RS can inject L0 accepts at regular intervals, i.e. every *n* turns at a specifiable bunch crossing. The periodic L0 accepts can optionally be marked such that keeping the corresponding L1 triggers is guaranteed. If the periodic trigger is used in stand-alone running, an internal mechanism emulates the latency of the L1 triggers.
- **Trigger pattern**. The RS can repeatedly produce a programmable pattern (3564 steps long) of L0 triggers. Optionally, the L0 accepts can either all be kept at Level-1 or all be rejected.
- **Periodic set of consecutive triggers.** The RS can inject a set of up to 16 consecutive L0 accepts

[6] This is an entirely artificial number. The maximum is actually 40 MHz…

at regular intervals, i.e. every *n* turns, starting at a specifiable bunch crossing.

- **Single-shot triggers.** Via the ECS a single L0 accept can be injected by writing the bunch crossing number to accept. Optionally, the L0 accept can either be kept or rejected at Level-1. For test purposes there is also the possibility to transmit a single L1 trigger with any trigger qualifier.
- **Single-shot of consecutive triggers.** Via the ECS a programmable set of consecutive L0 accepts can be injected by writing the number of triggers and the number of the bunch crossing to start. Optionally, the L0 accepts can either be kept or rejected at Level-1.
- **Spy triggers**. Several Readout Supervisors will be interfaced to the central triggers. This means that a test of a sub-detector partition can use the physics triggers to trigger its readout in a spying mode without actually participating to or interfering with the central readout.
- **External trigger**. The Readout Supervisor has an auxiliary L0 trigger input for connecting any optional external source of L0 triggers. The Readout Supervisor can either be programmed to keep or reject all auxiliary triggers at Level-1.

Spying on physics triggers is referring to the L0 trigger only. The Readout Supervisor generates internally a L1 trigger accept for each L0 trigger accept. Obviously, this will in normal circumstances lead to a rate that cannot be handled by the L1 Front-End electronics. However, either the L1 rate is self-regulated by the throttle mechanism, or the L0 trigger rate can be downscaled in the Readout Supervisor.

To the extent that it makes sense all the functions above can be combined. If L0 triggers from two different sources conflict a fixed priority scheme determines the definition of the trigger.

5.6 Time aligning a detector

Time alignment consists of a gross tuning at the level of 25 ns and a fine-tuning at the level of 100 ps[10]. The first is aimed at adjusting the TTCrx such that the bunch crossing ID, the L0 pipeline, the arrival of the data, and the arrival of the L0 trigger are synchronised. For this purpose the TTCrx can delay the TTC signals up to 16 clock cycles. It may also include adjusting an offset to the local bunch crossing counter where applicable. Provided no other changes are made to the system, it should in principle be sufficient to perform this alignment once and for all during the commissioning.
The fine-tuning is in order for the detector electronics to sample the signal at the optimal point. It is carried out by means of the fine adjustment provided by the TTCrx if nothing else is foreseen by the sub-detector. The TTCrx allows adjusting the TTC signals by 250 steps of 100ps. However, mind that it is not possible to maintain a timing alignment within 100ps! There are several contributions to large uncertainties. In additon, the exact level and behaviour of these contributions are not known. The values presented here should only be used as indicators of the order of magnitude:

- Bunch length: 257ps (RMS) at a time scale of bunch to bunch.
- Longitudinal phase stability of each bunch: 300ps (RMS) at a time scale of LHC turns.
- Drifts due to temperature variations of the TTC fibres from SR4 (location of LHC timing generators) to LHCb (~10km): 200ps at a time scale of 24 hours.
- TFC distribution network: 100 - 200ps using different Readout Supervisors.
- TTCrx temperature variation: 70ps/^{o}C.
- Effects of temperature on detector and detector electronics.
- Clock jitter at the output of the TTCrx: 100 – 150 ps (RMS) using Channel B to 100%.

Therefore, it is important to strive to achieve wide signal plateaus and make timing alignments routinely in order to maintain optimal sampling.

Timing alignment is done using the LHC bunch crossings and can be performed with all sub-detectors together or in stand-alone mode. It is achieved by accepting sets of consecutive bunch crossings around an isolated bunch interaction. The L0 Decision Unit will have a special algorithm to evaluate several consecutive crossings and will signal the Readout Supervisor ahead in order to force a number of triggers before and after an isolated bunch interaction.

Since the timing alignment utilises the L0 Decision Unit, aligning a detector stand-alone implies using the spying mode for triggering, as described above.

The L0 triggers are forced at Level-1 and the L1 trigger qualifier allows the L1 timing alignment triggers to be recognised.

5.7 Detector Calibration

Calibrations to measure electronics noise and determine pedestals and thresholds etc, will generally be performed without beam in stand-alone running. This involves reserving the sub-detector (partition elements) and a Readout Supervisor for stand-alone running, and downloading via the ECS interface whatever special configuration is needed in the Front-End electronics. The Readout Supervisor can then be configured to provide any of the triggering schemes listed in Section 5.4. The design of the Front-End electronics determines whether the calibration data is read out directly using the ECS interface on the Front-End electronics or if the calibration data is pushed through the entire DAQ system.

Calibrations may also involve generating data within the electronics or firing a pulse in the detector. For this purpose there is also a function to send in a programmable sequence a TFC control command (user bits: 0001XX00) to trigger the calibration system and after some programmable delay inject a L0 accept trigger. The triggers are automatically marked such that keeping them at Level-1 is guaranteed. The function allows specifying the periodicity and the number of the bunch crossing at which to send the calibration command. The bits XX allows to differentiate several calibration commands if needed[7].

If several detectors use the same command to fire their calibration system, a common latency has to be defined between sending the command and generating the L0 accept. However, different calibration systems normally have different response times. It will therefore be necessary to introduce adjustable delays in the Front-End electronics between the decoding of the calibration command and actually firing the calibration pulse[10].

It may also be of interest to monitor the calibration parameters during physics data taking. Therefore, all the functionality above is available and can be adjusted such that the monitoring triggers correspond to bunch crossings without beam or with single beam in case beam related noise is suspected. In case the monitoring triggers should be recognised and handled by the Front-End electronics, the Readout Supervisor can tag them using the L1 trigger qualifier.

[7] This has still to be defined.

As described in Section 4, when a partition is requested, also the purpose of the partition must be specified. The purpose will also determine which components are configured and added to the partition. For instance a calibration run of a sub-detector may only involve the Front-End electronics and not the entire DAQ chain. However, if special processing of the calibration data is required, the data must be passed to the sub-farm. In this case, the necessary DAQ components will be added to the partition. In addition they may be configured in a way that the data is passed to only specified destinations in the sub-farm where the special processing runs.

5.8 Physics Data Taking

In normal physics data taking all sub-detectors are in the global partition and one Readout Supervisor controls them all. To the extent that it makes sense, all the functionality described above is available. The "central RS" can be configured to transmit electronics resets and to auto-generate triggers for calibration and monitoring during the LHC bunch gaps. However, note that there is only one RS driving all the sub-detectors. Consequently, the Front-End electronics of the sub-detectors must conform to the specifications in a way that all the necessary functionality can be defined and set up in a global and common manner.

If a detector starts misbehaving, the run has to be stopped and if the problem can not be immediately solved, the detector is taken out of the global partition. It can then be debugged and tested separately in parallel to the physics data taking as described in Section 5.4.

5.9 Special test functions

In addition to the functionality described above, a few special functions are implemented:

- **"L0 timed run"**. The Readout Supervisor starts a run and continues until a programmable number of L0 triggers have been accepted.
- **"L1 timed run"**. The Readout Supervisor starts a run and continues until a programmable number of L1 triggers have been accepted.
- **Manual throttling.** The operator can throttle the L0 and the L1 triggers via the ECS.
- **Manual electronics reset.** The operator can fire the L0 and the L1 electronics resets via the ECS by specifying the number of the bunch crossing at which it shall take place.

6 Summary of Functions and Parameters

Function	Parameters
Single-shot L0 trigger	• Bunch crossing
Single-shot L1 trigger	• L1 trigger qualifier • Bunch crossing
Single-shot TFC control command	• Control command • Bunch crossing
Single-shot set of L0 (and L1) consecutive triggers	• Number of triggers • Bunch crossing • L0 trigger: always kept at Level-1 (on/off)
Random L0 trigger	• Activate (on/off) • Rate
Random L1 trigger	• L0 random trigger always kept (on/off) • Activate random L1 triggers (on/off) • Rate
Periodic L0 (and L1 trigger)	• Periodicity • Bunch crossing • Always kept at Level-1(on/off)
L0 (and L1) trigger pattern	• Pattern (3564 bits) • Always kept at Level-1(on/off)
Periodic set of consecutive L0 (and L1) triggers	• Periodicity • Bunch crossing • Number of triggers
L0 and L1 spy triggers	• Use reserve RS connected to L0 and L1 decision units
Auxiliary L0 (and L1) triggers	• Activate auxiliary L0 input (on/off) • Always kept at Level-1(on/off)
Timing alignment triggers	• Number of triggers
Periodic calibration pulse and L0 (and L1) trigger	• Periodicity • Bunch crossing • Calibration pulse type • Always kept at level-1(on/off)
L0 timed run	• Number of L0 triggers
L1 timed run	• Number of L1 triggers
Manual L0 throttling	• Activate (on/off)
Manual L1 throttling	• Activate (on/off)
Manual L0 electronics reset	• Bunch crossing
Manual L0+L1 electronics reset	• Bunch crossing
Start data taking (release L0 trigger)	• Activate (on/off)
Start data taking (release L1 trigger)	• Activate (on/off)

7 Performance Statistics and Run Information

The RS keeps a large set of counters that record its performance and part of the performance of the data-taking (dead-time etc.).

Table 2 lists the most important monitoring information. The counters are also gated with the throttle signals (due to imminent buffer overflow, during electronics resets etc) in order to compute the dead-times.

Table 2: The most important statistics counters by the Readout Supervisor.

Counter
LHC bunch crossings
LHC orbits
Bunch crossing number
L0 accept triggers (all different types and total) → L0 Event ID
L0 accept triggers marked to be kept at Level-1 (all different types and total)
L1 trigger decisions
L1 accept triggers (normal, random and total) → L1 Event ID
L0 synchronisation errors (L0 Decision Unit – RS)
L1 synchronisation errors (L1 Decision Unit – RS)
L0 trigger throttles (all different types and total)
L1 trigger throttles (all different types and total)

The RS also incorporates a series of buffers analogous to a normal Front-End chain to record local event information and provides the DAQ system with the data on an event-by-event basis. The "RS data block" contains together with status information, the "true" bunch crossing ID and the Event Number, and is merged with the other event data fragments during the event building.

8 References

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