- 17 months

TFC Tutorial

Introduction 1

- Aim with tutorial
  - Introduce setting up and operating TFC system for detector tests
  - Show an example of the implementation of a complete local control system
  - Divided in two parts:
    - “Theoretical” and ‘live demonstration’
  - Feedback and discussion on needs

- What I will not talk about…
  - Other TFC components than Readout Supervisor ‘ODIN’ and Throttle OR ‘HUGIN’
  - How to set up Credit Card PC infrastructure (Niko)
  - How to install PVSS
  - How to set up and operate the TELL1
  - How to operate ODIN in the pit

- Reservation
  - Transition period L0+L1 → only L0 with ODIN and TELL1
  - Things are in evolution…
  - My colleague Murphy…

Introduction 2

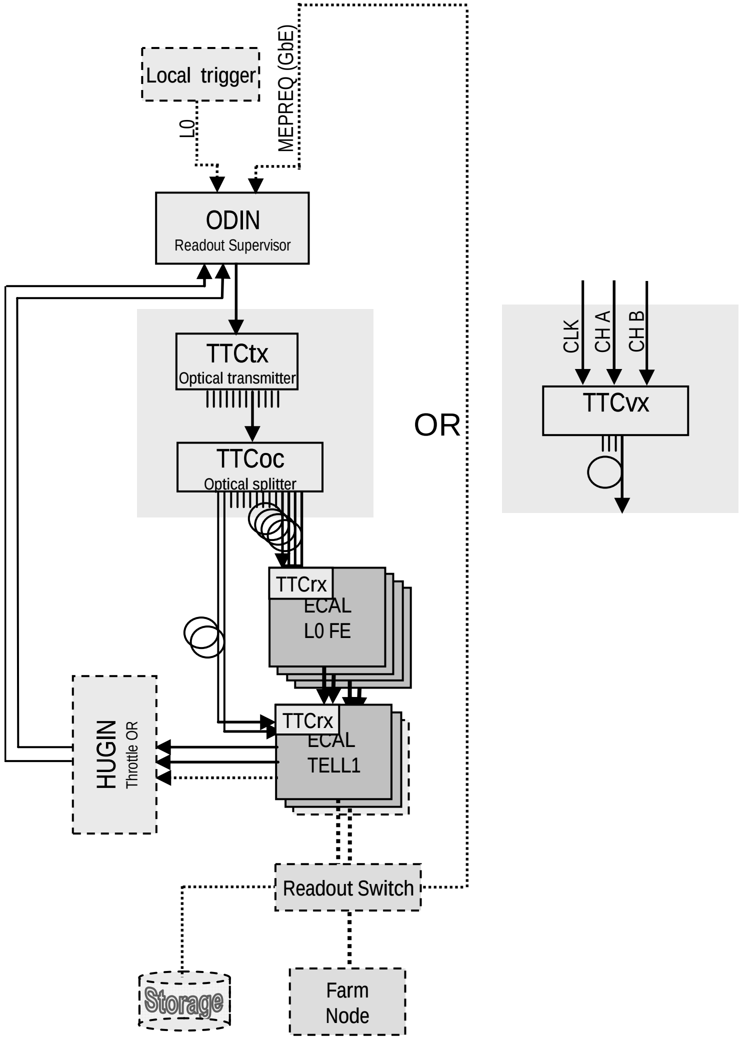
- What I will talk about:
  - Typical Detector Test Setup
  - TFC Functionality needed in local tests
  - ODIN Hardware
  - ODIN I/O Interfaces
  - ODIN Low-level Control
  - TFC Local Control System (PVSS)
  - TFC Hardware Installation Demo (ODIN and mention HUGIN)
  - TFC Local Control System Demo
  - TFC LC Installation Demo
  - Getting Equipment and Support

Detector Test Setup

- LHCb components:
  - Readout Supervisors ('ODIN')
  - Throttle Ors ('HUGIN')

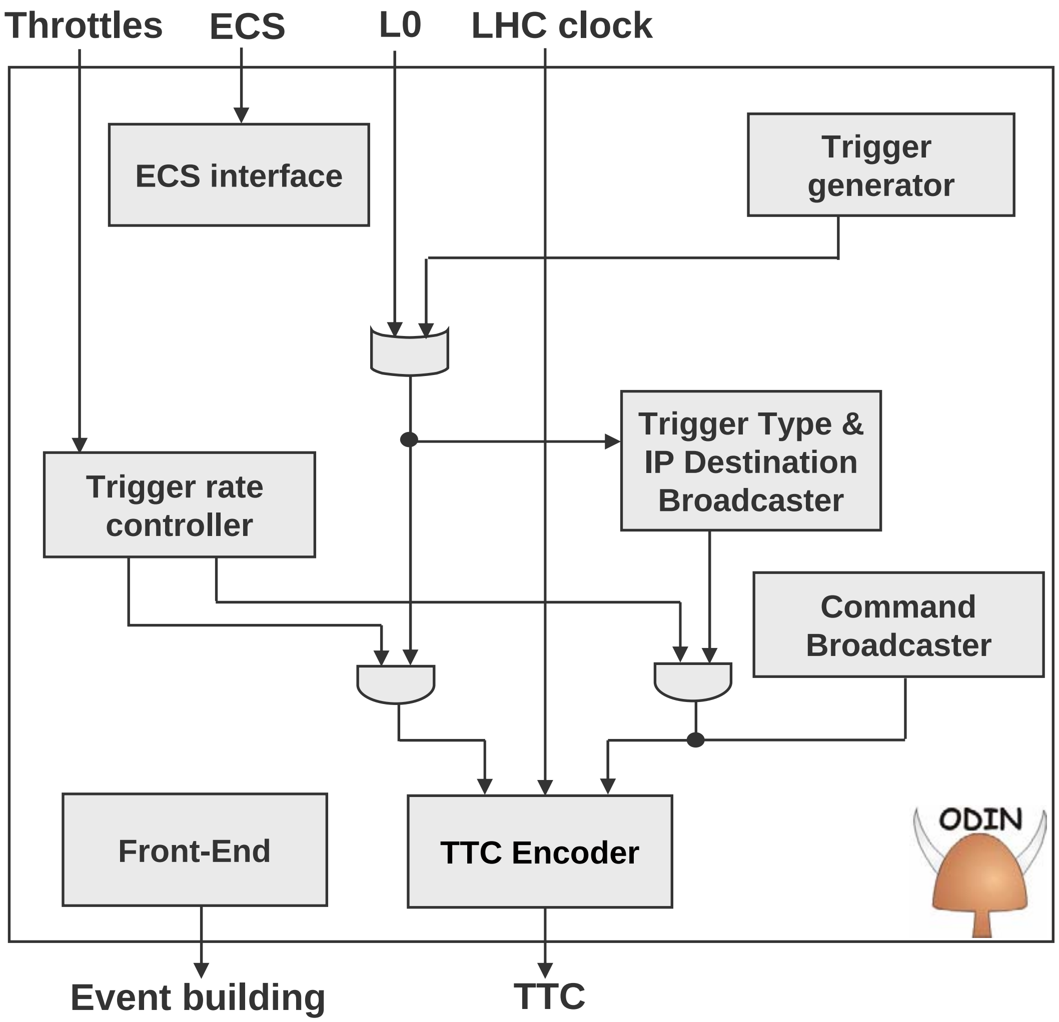
- TTC components
  - TTCtx (electrical-optical converter)

    Alternatively
  - TTCvx (encoder & optical transmitter)
  - TTCoc (optical fan-outs)
  - Attenuators



ODIN Functional Block Diagram

- I will talk about:
  - Clock and orbit
  - Auto-trigger generator
  - External triggering
  - Trigger handling
  - Trigger rate control
  - Command generator
  - (ODIN Front-End)



ODIN Heartbeat(s)

- Bunch clock
  - Two sources: External ECL AC coupled and internal ECL VXCO 80.158 MHz
  - PLL clock driver for 40MHz, 80MHz, 160 MHz (MPC991 obsolete)
  - Source selected by I^{2}C
  - (Fine phase adjustment for global alignment :2.2 – 12.2ns in 10ps steps…)
  - Bunch clock output for TTCvx or trigger or… (ECL AC coupled)
- Orbit (sometimes called turn/revolution) signal
  - Two sources: External ECL DC coupled and internal generated in FPGA from BCLK
  - Source selected by the same I^{2}C control line as for the bunch clock
  - In internal mode, orbit length is configurable… (P_ORBIT_LEN = 128 - 3563)
- Bunch Counter Reset (BCR) broadcasting
  - Always as soon as orbit length is configured (internal) or external orbit signal present (external)
  - Currently no other command comes together with the BCR broadcast

L0 Trigger Sources

- Internal trigger sources
  - Random trigger
  - Periodic trigger
  - Trigger sequence
  - Calibration trigger
  - (Timing trigger)

- External trigger sources
  - Physics trigger
  - Auxiliary trigger

- Random trigger
  - Requires two 32-bit random seeds (loaded on enabling random generator)
  - Generates two uniform 32-bit random number every clock cycle
  - Trigger rate adjusted by threshold: rate(L0) = 40 MHz * (1- (threshold / (2^{32} – 1)))

- Periodic trigger
  - Two periodic trigger generators (A and B)
  - Generates single burst of consecutive triggers at programmable bunch crossing every *n* orbits
  - Programmable: burst length (<16), offset (0 – 3563), periodicity (24 bits)
  - Special: rate may be increased by shortening orbit length

L0 Trigger Sources

- Trigger sequencer
  - Repeat programmable trigger sequence of up 3564 bunch crossings

- Calibration trigger
  - Three calibration trigger generators (A, B and C)
  - Calibration generator A is set up with common calibration command (000100XX)
  - Sequence:
    - Send calibration command at programmable bunch crossing (offset) every *n* orbits (periodicity)
    - Wait programmable delay before generating L0 trigger (normally 160+16)
  - Calibration command for B and C may (*will*) be programmable (Currently 101 and 110, resp.)
  - If calibration may not be sent due to clash with command of higher priority -> Repeated at the same crossing in the next orbit
    - Status bit is indicating “Repeat attempt”
  - Special: rate may be increased by shortening orbit length

L0 Trigger Sources

- External L0 Trigger Input (Physics)
  - Parallel 16-bit LVDS with twisted pair flat ribbon cable and 3M HE-10 connectors
    - Pin configuration in ODIN Technical Reference
  - Attention: Must be disabled if nothing is connected, otherwise L0 triggers at 40 MHz!
  - Normally synchronization check is performed on received Bunch ID
    - Must be disabled if no proper Bunch ID

15	14	13	12	11 .. 0
Reserve	L0_TIM_TRG	L0_FORCE	L0_DECIS	L0_BID

- Auxiliary L0 trigger input
  - Single-ended ECL DC-coupled via LEMO
  - Edge detect at input
  - ODIN generates burst of consecutive triggers (programmable length <16) on pulse
  - Pipeline of programmable length for additional adjustment of latency
  - Random generator may be used to take random decisions for the auxiliary triggers

L0 Triggers

- Current allocation of trigger types
  - Will soon change
  - Priority scheme decides trigger type if coincidence

Trigger type	Encoded	Priority
Reserve	000	-
Physics trigger	001	1
Auxiliary trigger	010	2
Random trigger	011	3
Periodic trigger	100	4
Trigger for non-zero suppressed data**	101	-
Timing trigger	110	5
Calibration trigger	111	6

- Additional features for L0 triggers
  - Single shot of any trigger generator via control system
    - Will generate trigger (-sequence) according to specified timing (offset, burst length etc) in next orbit
  - “Timed running” : Max number of L0 triggers
    - Automatic stop after programmable number of L0 triggers (any source)
  - L0 Event ID counter reset broadcast (ECR)
    - Sent together with BCR at programmable periodicity (24 bits)
    - Single shot via control system (always together with next BCR)
  - All functions may be enabled/disabled

- Attention!:
  - Programmable parameters may still have an undocumented “+/-1”

Trigger Rate Control

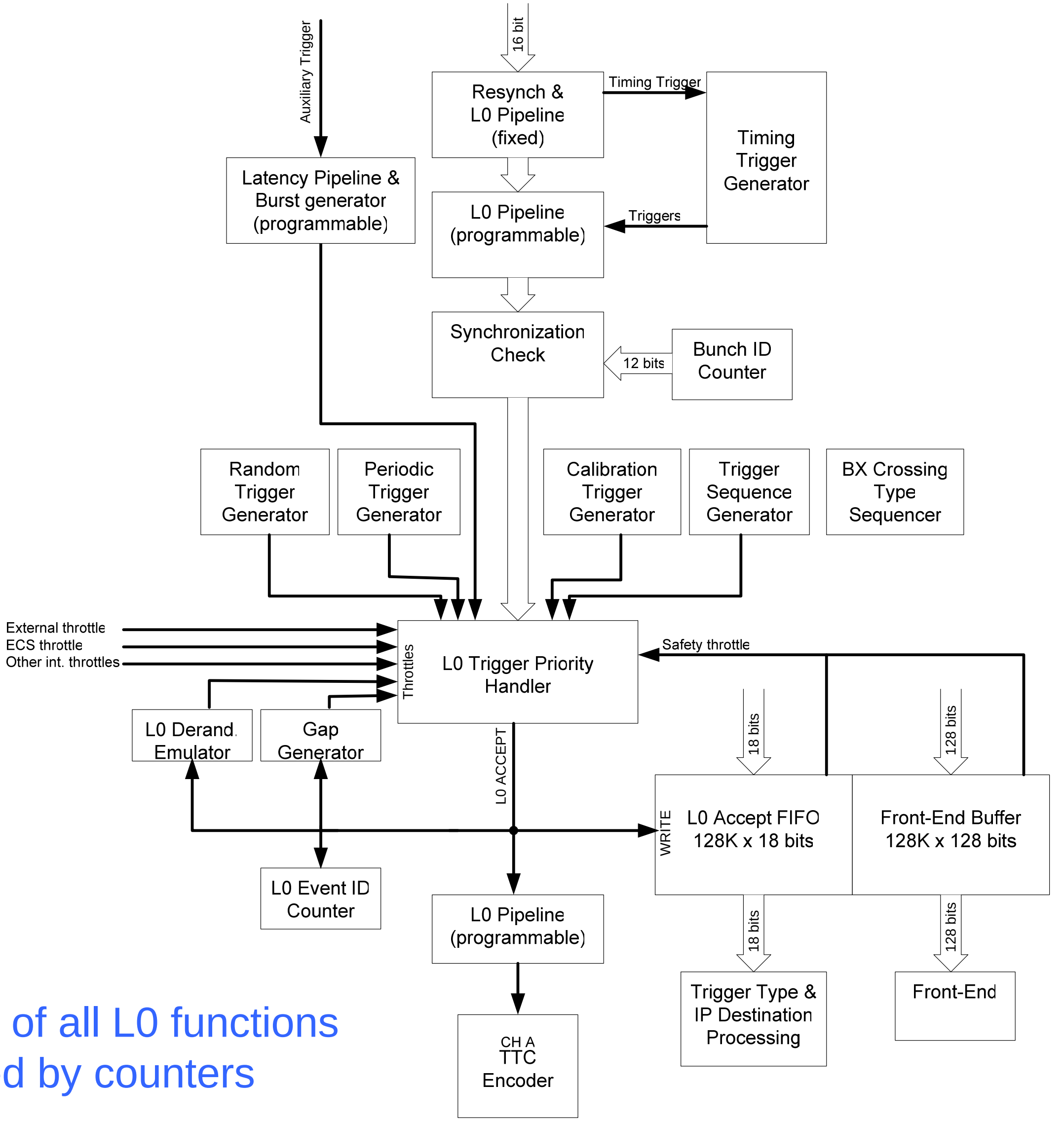
- L0 throttle sources
  - External L0 throttle
  - L0 derandomizer emulator
  - Gap generator
  - L0 Electronics Reset
  - L1 Electronics Reset
  - (ECS throttle)
  - (L0 Accept FIFO safety throttle)
  - (Front-End Buffer safety throttle)
  - Automatic L0 trigger stop (Max number of triggers)

- L0 throttle inputs
  - Two connector for two TELL1
  - Dual twisted pair LVDS with RJ9 connectors
  - Attention : Must be disabled if nothing connected, otherwise permanently on

L0 Trigger Rate Control

- L0 derandomizer emulator
  - Emulates occupancy of L0 derandomizer
    - Throttles at programmable upper water mark and releases triggers at lower water mark
  - Requires configuring L0 readout time (typically 36 cycles)
- Gap generator
  - Introduces a forced gap of programmable length between L0 trigger accepts
- L0 Electronics Reset
  - L0 triggers are throttled until derandomizer is empty and until L0 Electronics Reset is ready
- L0+L1 Electronics Reset
  - L0 triggers are throttled during the L0+L1 Electronics Reset
- All functions may be enabled/disabled

L0 Trigger Processing


Auxiliary Trigger
16 bit
Resynch & L0 Pipeline (fixed)
Timing Trigger
Timing Trigger Generator
Latency Pipeline & Burst generator (programmable)
L0 Pipeline (programmable)
Triggers
Synchronization Check
12 bits
Bunch ID Counter
Random Trigger Generator
Periodic Trigger Generator
Calibration Trigger Generator
Trigger Sequence Generator
BX Crossing Type Sequencer
External throttle
ECS throttle
Other int. throttles
Throttles
L0 Trigger Priority Handler
Safety throttle
18 bits
128 bits
L0 Derand. Emulator
Gap Generator
L0 ACCEPT
WRITE
L0 Accept FIFO 128K x 18 bits
Front-End Buffer 128K x 128 bits
L0 Event ID Counter
L0 Pipeline (programmable)
18 bits
128 bits
Trigger Type & IP Destination Processing
Front-End
CH A TTC Encoder

- The activity of all L0 functions are recorded by counters

TTC Commands

- TTC Commands:
  - L0 Front-end electronics reset
  - L0+L1 Front-end electronics reset
  - Periodic command
  - IP Destination broadcast

	7	6	5	4	3	2	1	0
Trigger Type	1	Trigger type			L0 EvID		(ECR)	(ECR)
Reset	0	1	R	R	L1 FE	L0 FE	ECR	BCR
Calibration	0	0	0	1	Pulse type		(ECR)	(BCR)
Command	0	0	1	Command type			(ECR)	(BCR)

- L0 Front-End electronics reset
  - Sequence
    - Throttle the L0 triggers until L0 derandomizer is empty Broadcast L0 electronics reset command
    - Release the L0 triggers when front-end electronics is fully operational
  - Programmable parameters:
    - Periodicity (24-bits)
    - Bunch crossing at which sequence starts (offset)
    - Throttle time (typically 576 cycles)
    - Delay to release triggers

TTC Commands

- L0+L1 Front-end electronics reset
  - Sequence (Not fully decided)
    - Throttle L0 triggers (Flush MEP buffer in TELL1?)
    - Send L0+L1 electronics reset
    - Release triggers when L0 and L1 electronics is fully operational
  - Programmable parameters:
    - Periodicity (24-bits)
    - Bunch crossing at which sequence starts (offset)
    - Delay to release triggers

- Periodic command
  - Used to transmit a programmable user command (Any TTC short broadcast)
  - Programmable parameters: Periodicity, offset, user command (8-bits)

TTC Commands

- Additional features:
  - Single shot of any trigger generator via control system
    - Will generate sequence according to specified timing (offset, burst length etc) in next orbit
  - Priority scheme decides if commands coincidence
  - If command may not be sent due to clash with command of higher priority -> Repeated at the same crossing in the next orbit
    - Status bit is indicating “Repeat attempt”
  - All functions may be enabled/disabled
  - Special: rate may be increased by shortening orbit length

- Remark:
  - Ensure that commands don’t clash by setting the offsets properly
    - A command cannot be sent <17 cycles before another short broadcast and not 42 cycles before long broadcast
  - Programmable parameters may still have an undocumented “+/-1”

IP Destination Assignment

- Two schemes for IP Destination assignment in local tests
  - Static round-robin
  - Dynamic based on “MEP Requests” by farm nodes via GbE
    - Not yet implemented in farm software

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP destination	1	0	Flush	R	Ethernet/IP address											

- Configuration of IP Destination Assignment:
  - IP Destination table loaded via ECS in both cases
  - Configure packing factor

- Flush broadcasts is generated on demand via control system

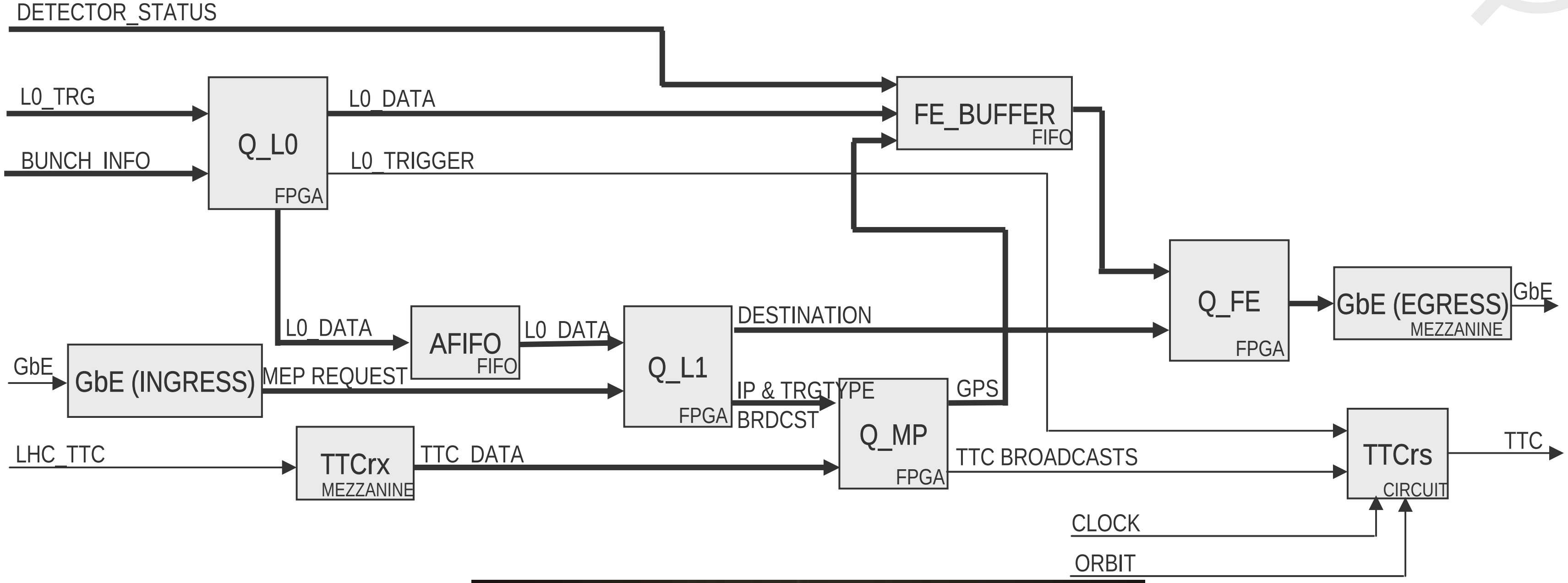
Other features

- TTC Encoder on board
  - Output is multiplexed A/B channel ECL AC-coupled (use with TTCtx)

    Or
  - Channel A and B separately (use with TTCvx or TTCex)

- (Detector status)
  - 2-bit status information from each detector, for instance
    - 1-bit HV on/off
    - 1-bit encoding status of other systems which indicates that detector is fully operation for data taking
  - LVDS signal
    - Parallel 24-bit LVDS with twisted pair flat ribbon cable and 3M HE-10 connectors
    - RJ45 cable from detector

ODIN Dataflow

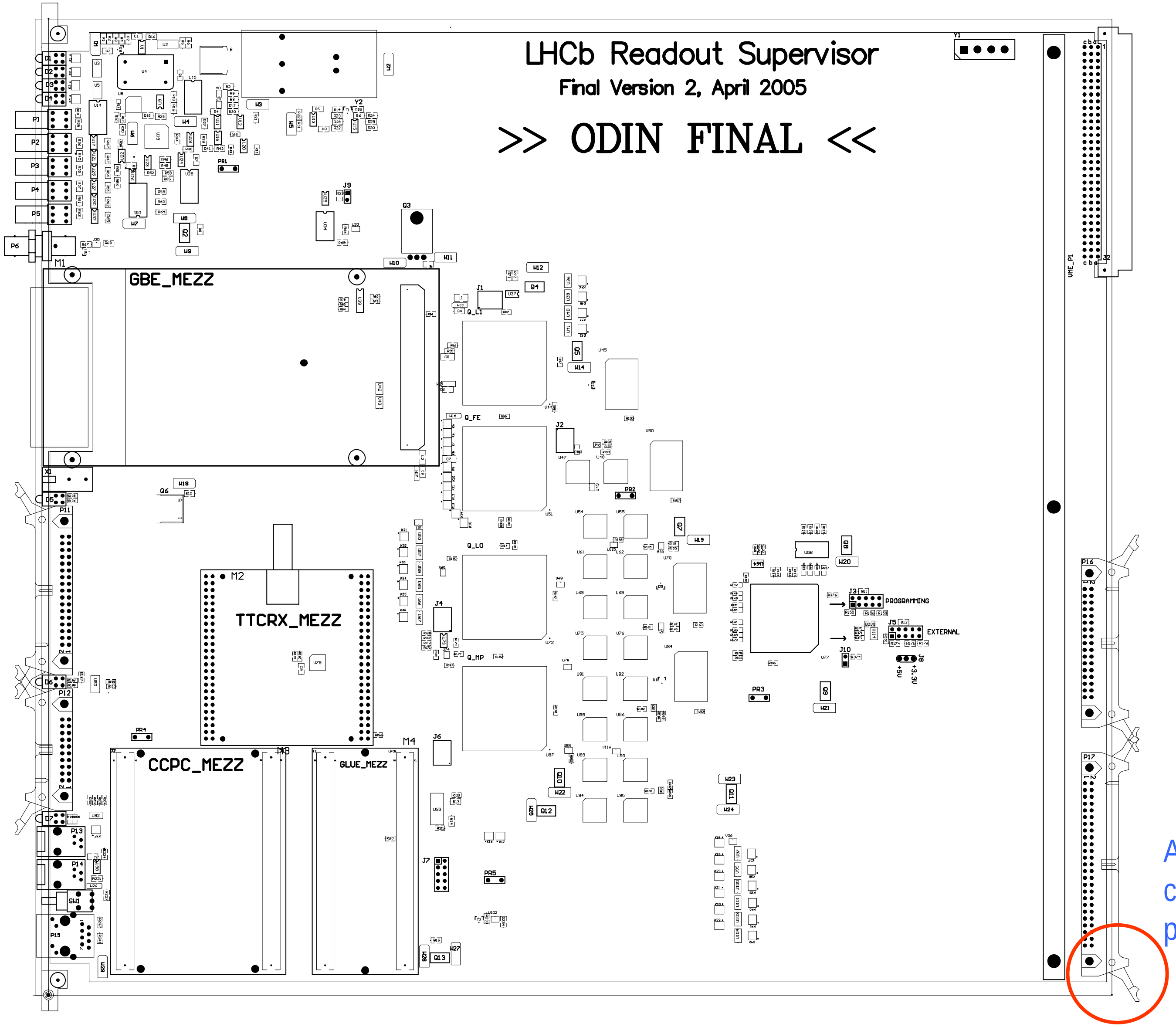


Hardware

- Mechanics
  - 9U VME
  - Same backplane as TELL1/UKL1
  - Holes for rigidity bar (only one backplane connector) (not yet mounted)
  - Front panel not yet mounted
- Board power
  - Use only +5V ➔ -5V, 3.3V, 2.5V and 1.8V made on board
    - Total 6.4A@5V (“idle”) / <9A@5V (“full operation”)
  - Require cooling but can survive for periods without
  - Back plane / PC power connector
  - Power monitoring circuit
    - Range 4.7 V – 5.3 V
    - LED and status bit in FPGA
- Manual reset of CCPC + Glue
  - Back plane (Attention: Problems observed with backplane reset on some TELL1 crates!)
  - Reset button
- Jumpers and test pads
  - None have to be touched to operate ODIN

Jumper	Function
J1	Q_L1 test pad (pins 0 and 1)
J2	Q_FE test pad (pins 0 and 1)
J3	JTAG header for programming of JTAG hub
J4	Q_L0 test pad (pins 0 – 8)
J5	External JTAG master source
J6	Q_MP test pad (pins 0 – 11)
J7	RS232 interface to CCPC
J8	Voltage selection for external JTAG master
J9	Write protection for board identifier
J10	Reserve control input for JTAG hub

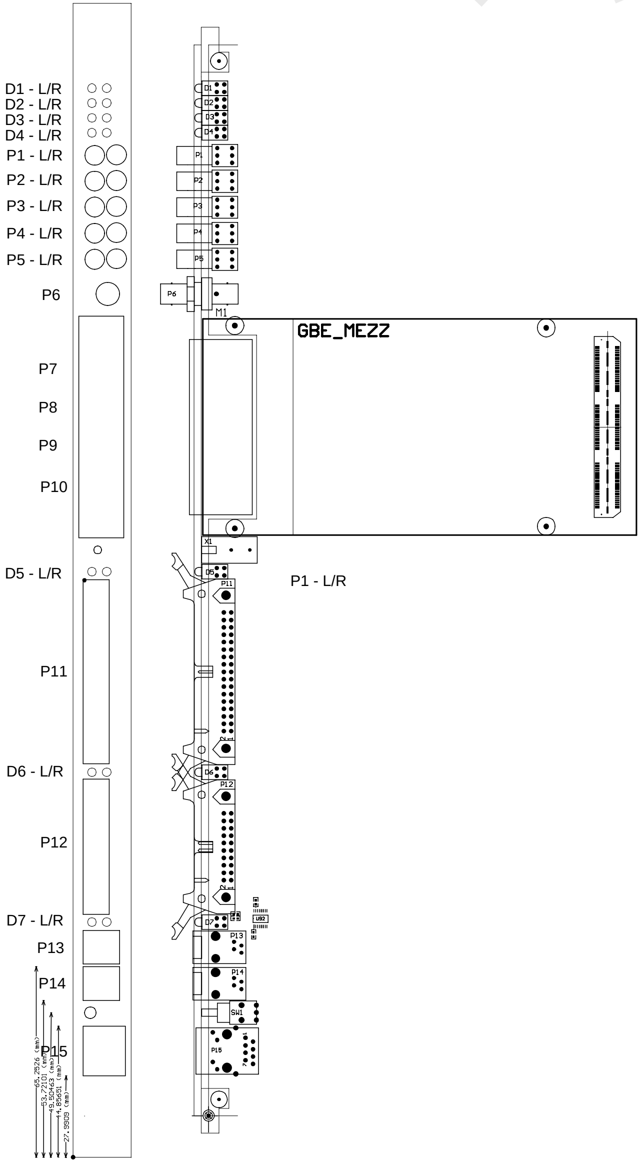
Hardware



Attention: rear connector clips when plugging in crate

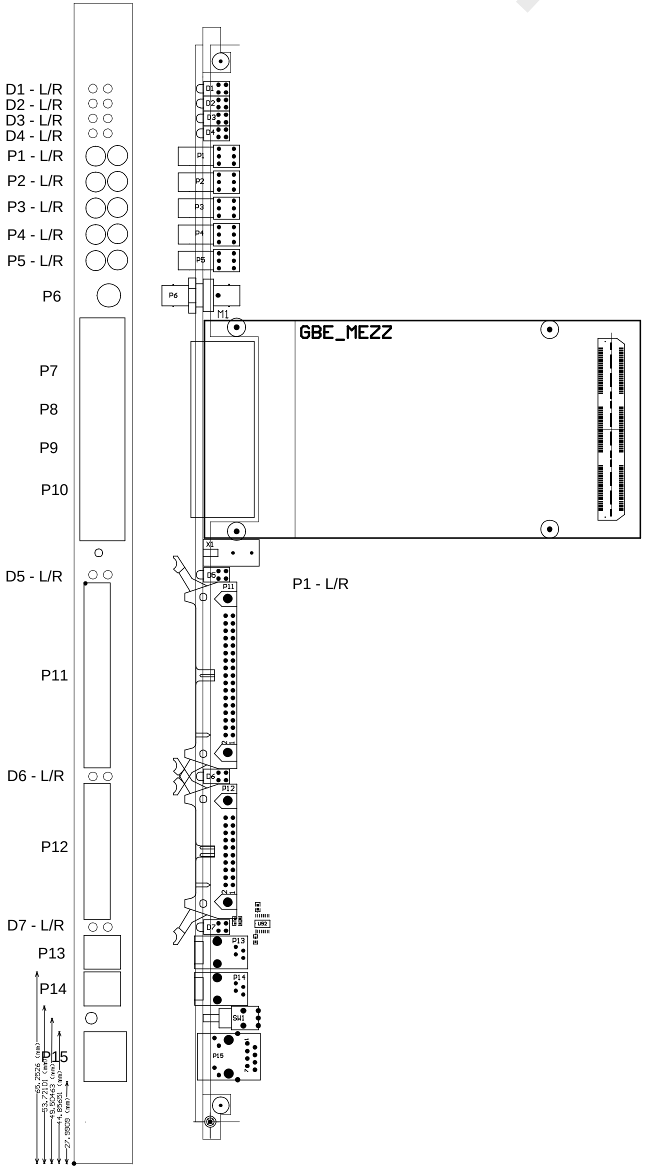
Status LEDs

Designator	Function	Normal Activity		Abnormal Activity	
D1-L	Power Supply Status	Power OK	Green	+5V Out of Range	Blinking Red
D1-R	System Reset	OFF	Green	ON	Red
D2-L	All FPGA's Configured	Yes	Green	No	Red
D2-R	PLL Locked	Locked	Green	Unlocked	Red
D3-L	External Orbit Present	Yes	Green	No	Red
D3-R	External Clock Present	Yes	Green	No	Red
D4-L	BCLK & Orbit Selection	External	Green	Internal	Red
D4-R	L0 Sync Error	No	Blank	Yes	Red
D5-L	L1 Accepts Present	Yes	Green	No	Blank
D5-R	L1 Sync Error	No	Blank	Yes	Red
D6-L	Reserve	Yes	Green	No	Blank
D6-R	L0 Accepts Present	Yes	Green	No	Blank
D7-L	L0 Throttle Present	No	Blank	Yes	Red
D7-R	L1 Throttle Present	No	Blank	Yes	Red



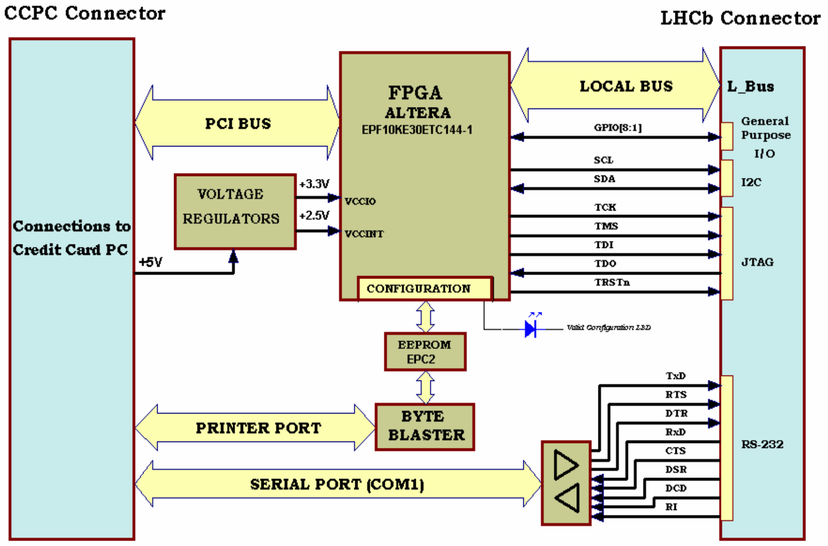
I/O Interfaces

Designator	Function	Mode	Signal	Location	Connector
P1-L	Orbit	In	DC ECL	Front Panel	Dual LEMO
P1-R	Orbit	Out	DC ECL	Front Panel	Dual LEMO
P2-L	Bunch Clock	In	AC ECL	Front Panel	Dual LEMO
P2-R	Bunch Clock	Out	AC ECL	Front Panel	Dual LEMO
P3-L	TTC Channel A+B	Out	AC ECL	Front Panel	Dual LEMO
P3-R	TTC Channel A+B	Out	AC ECL	Front Panel	Dual LEMO
P4-L	TTC Channel A	Out	DC ECL	Front Panel	Dual LEMO
P4-R	TTC Channel B	Out	DC ECL	Front Panel	Dual LEMO
P5-L	Auxiliary Trigger	In	DC ECL	Front Panel	Dual LEMO
P5-R	Reserve	In	TTL	Front Panel	Dual LEMO
P6	BST Info	In	Optical	Front Panel	ST/PC
P7-P10	L1 Trigger	In	GbEthernet	GbE Mezzanine	RJ45
	DAQ	Out	GbEthernet	GbE Mezzanine	RJ45
P11	L0 Trigger	In	LVDS	Front Panel	3M 34-pins
P12	Bunch Crossing Info	In	LVDS	Front Panel	3M 14-pins
P13(0)	L0 Throttle 1	In	LVDS	Front Panel	RJ9
P13(1)	L1 Throttle 1	In	LVDS	Front Panel	RJ9
P14(0)	L0 Throttle 2	In	LVDS	Front Panel	RJ9
P14(1)	L1 Throttle 2	In	LVDS	Front Panel	RJ9
P15	Ethernet CCPC	I/O	Ethernet	Front Panel	RJ45
P16	L1 Trigger	In	LVDS	Back Panel	3M 34-pins
P17	Experiment Status	In	LVDS	Back Panel	3M 50-pins
VME-P1	Power Supply	-	-	Back Panel	DIN96_M



Board Control

- Control Interface: CCPC and Glue *light*
  - Ethernet (Attention: Ethernet cable length!
  - I^{2}C bus
  - JTAG interface
  - JTAG hub control bus (GPIO lines)
  - Local Bus



- I^{2}C
  - Five devices:

Function	Chip	Peripheral address
Odin board identifier	24LC024	0xA0
Hardware settings	PCA9554	0x40
Clock adjustment	PCA9555	0x42
TTCrx configuration	TTCrx	0xEC
GbE mezzanine identifier	GbE	0xAE

- JTAG
  - FPGA programming and boundary scanning in-situ (I do all firmware upgrade remotely)
  - Fully configurable JTAG hub (programmed via header):

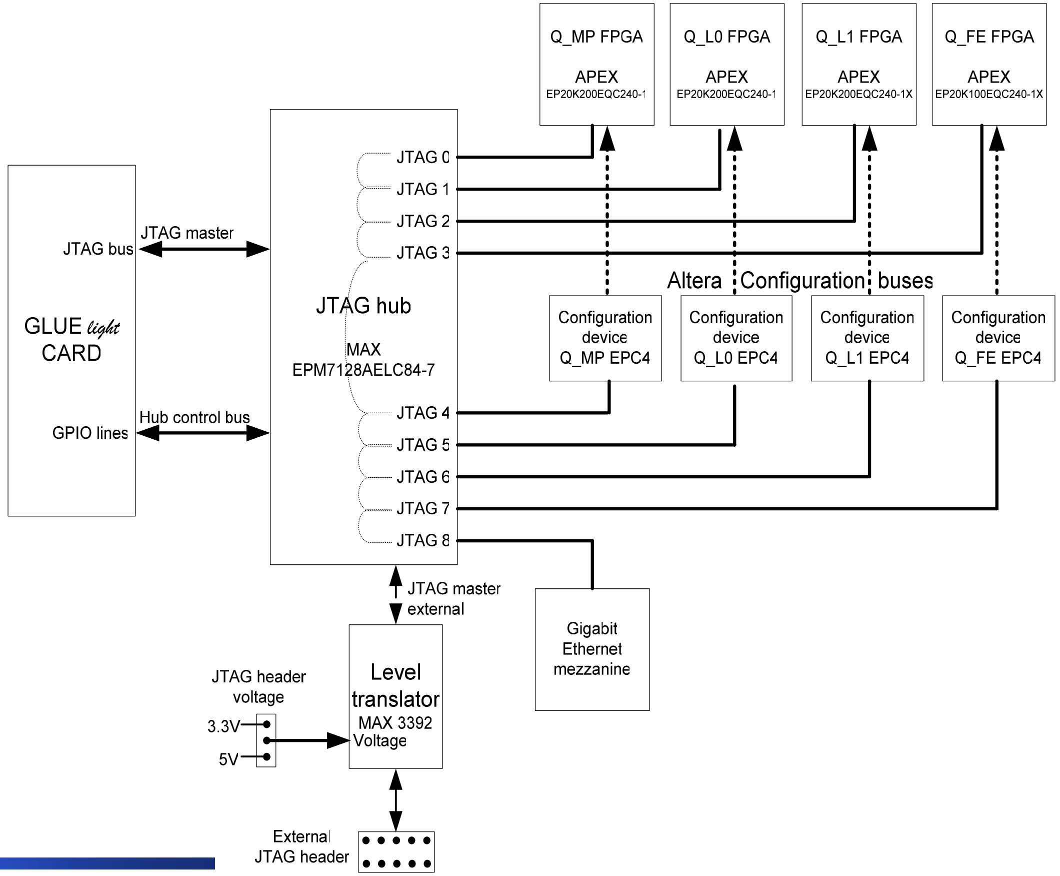
GPIO(7)	GPIO(6)	GPIO(5)	GPIO(4)	GPIO(3 .. 0)
LATCH	WRn	ADDR(0)	ADDR(0)	DATA(3 .. 0)

Board control

- JTAG hub registers

Register	Address	Bit 3	Bit 2	Bit 1	Bit 0
FPGA selection	“00”	Q_FE	Q_L1	Q_L0	Q_MP
EPC4 selection	“01”	EPC_FE	EPC_L1	EPC_L0	EPC_MP
Other	“10”	Ext/Int JTAG	Not used	GbE nTRST	GbE
Version (Currently 0xA)	“11”	1	0	1	0

- JTAG bus architecture



Board Control

- Local bus
  - Configuring, controlling and monitoring all TFC functionality in the FPGAs
  - PLX 9030 Local Bus specification:
    - 32-bit synchronous multiplexed address/data
    - Bus clock: system clock (BCLK) / 2 : ~20 MHz

Module	LBUS base address
Q_MP	0x1000
Q_L0	0x2000
Q_L1	0x3000
Q_FE	0x4000

- Resets and other hardware control lines:

Internal register	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Ouput port register (set out)	0x1	System reset	L1 Trigger LVDS	Encoder reset	Ext/Int System clock	Not used	Not used	Bunch info input	Detector status input
Port direction register	0x3	0	0	0	0	0	0	0	0

  - System reset set after power up

Board Control

- Board id and code version
  - Board identifier stored in I^{2}C EEPROM (0xA0)
  - Write protected

Board name	Revision	Number	SystemID(TFC)	BoardType	Revision	Serial number	Hex
			<31 .. 28>	<27 .. 20>	<19 .. 16>	<15 .. 0>	
OdinP2_00	P2	00	0010	00000000	0000	0000000000000000	0x20000000
OdinP2_01	P2	01	0010	00000000	0000	0000000000000001	0x20000001
OdinV1_00	V1	00	0010	00000000	0001	0000000000000000	0x20010000
OdinV1_01	V1	01	0010	00000000	0001	0000000000000001	0x20010001
OdinV2_00	V2	00	0010	00000000	0010	0000000000000000	0x20020000
OdinV2_01	V2	01	0010	00000000	0010	0000000000000001	0x20020001
OdinV2_02	V2	02	0010	00000000	0010	0000000000000010	0x20020002
OdinV2_nn	V2	nn	0010	00000000	0010	nn	0x2002xxxx

  - FPGA code version
    - Local bus: (Main FPGAs: base address + 0xFC / Glue *light* : 0x3C)
    - YEAR(4) : MONTH(2) : DAY(2) : “HOUR”(2), that is for instance 2005112800

Board Control

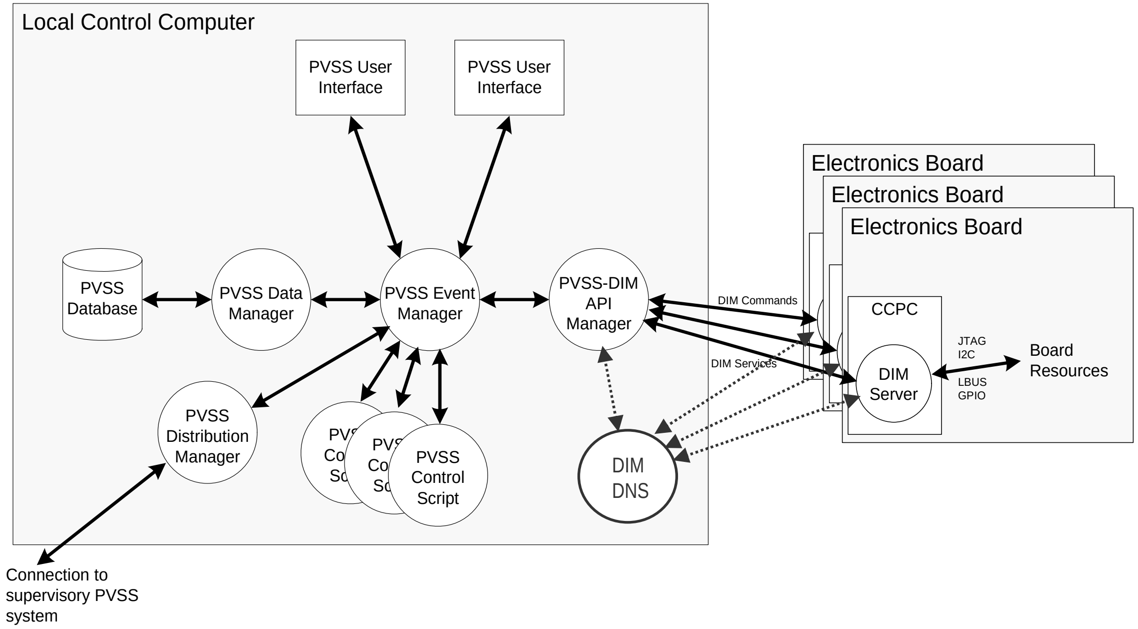
- TFC Control and Status registers
  - Local Bus registers in the main FPGAs
  - Configuration parameters (RW)
    - H_name : Hardware parameters linked to the actual installation (Set “once-only”)
    - P_name: Parameters configuring running modes and operation
    - R_name: Run related parameters which either enable/disable functions or operate the data taking
  - Status registers (RO)
    - S_name : Status bit for a particular function
      - Distinction _INSTantaneous and _CONTinuous
    - C_name : Counter register
    - D_name : Data register
  - Reset registers (RW)
    - RST_name : Reset bits resetting individual functions
    - RST_CNT : Global reset of all counters and instantaneous status bits
    - RST_SEL_CNT : Selective reset of individual counters
  - Action registers (WO and/or RO)
    - DMND_name : “Single-shot” bits to activate a function once on demand via ECS
    - UPDATE_CNT: Updates simultaneously all counter buffers for reading via ECS

Control software

- Low-level control on CCPC
  - System reset
    - `> sres`
  - I²C read/write
    - Read: `> i2c –r –i<internal register> <peripheral address>`
    - Write: `> i2C –w<value> -i<internal register> <peripheral address>`
  - Local bus read/write
    - Read: `> lbus –r <register>`
    - Write/read: `> lbus –w<value> <register>`
    - Write only: `> lbus –p<value> <register>`
  - JTAG hub control
    - Read: `> jtaghub –r <register>`
    - Write: `> jtaghub –w<value> <register>`
    - Reset: `> jtaghub -c`
    - `(> devsel <list of devices>)`
  - FPGA/EPC programming
    - `> jbi_pci –a<instruction>  Q_device.jbc`
  - Boundary scan
    - JTAG chain test and IDCODE: `> bscan –i<number of components>`
    - Boundary scan `> bscan –b<file.pat>`
  - Board status (Board name/identifier and firmware versions)
    - `> tstat`

TFC Local Control System

- Based on PVSS and DIM



- At CERN the control system is running on central control PC (PCTFCCTRL00)
  - Like in the final ECS
  - User only starts DIM server (TFC_server) on the board and the GUI

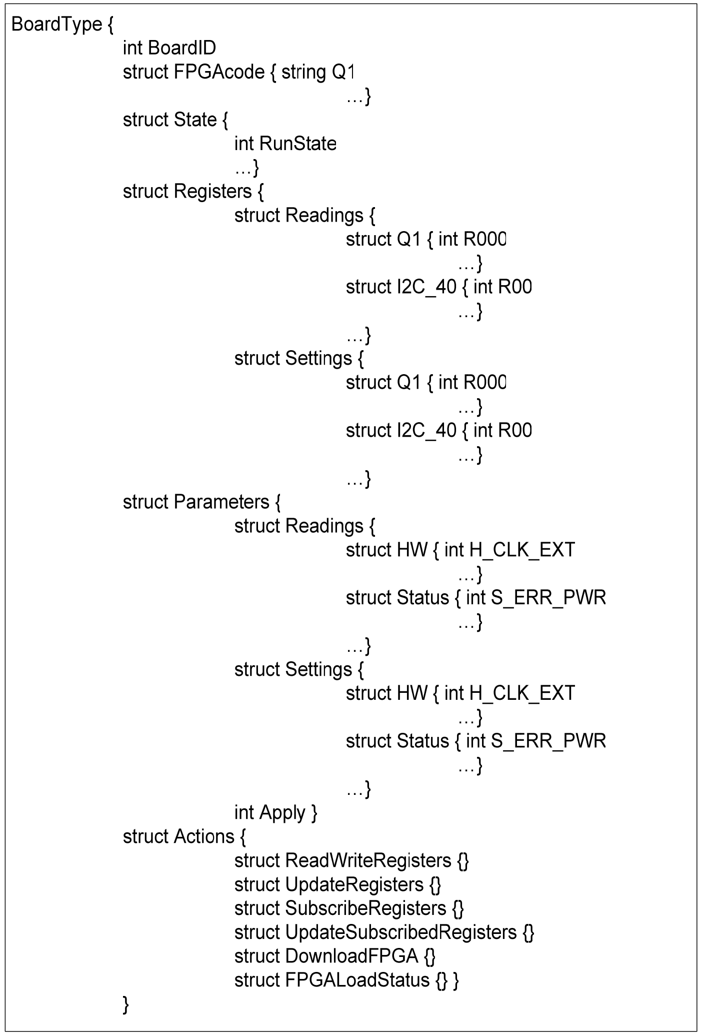
- I recommend running PVSS project on Linux machine and GUIs on Windows

TFC Local Control System

- TFC Server
  - All programming, control and monitoring via 3 DIM commands and 3 DIM services:
    - *ReadWriteRegisters (struct[] {method, address, data, mask, r/w})*
    - *UpdateRegisters (struct[] {address, data})*
    - *SubscribeRegisters(struct[] {address, interval})*
    - *UpdateSubscribedRegisters(struct[] {address, data})*
    - *DownloadFPGA(id, STAPL data)*
    - *FPGALoadStatus(id, status)*
  - Names of commands and services composed by reading Board Identifier at startup
    - E.g. /TFC/OdinV2_00/CMD/ReadWriteRegisters or /TFC/ThorV1_02/SVC/UpdateRegisters
  - Requires as argument the name of the DIM_DNS node
    - Normal: `> TFC_server pctfcctrl00.cern.ch`
    - Debug: `>TFC_server –d pctfcctrl00.cern.ch`
    - Don’t be surprised, four processes running

TFC Local Control System

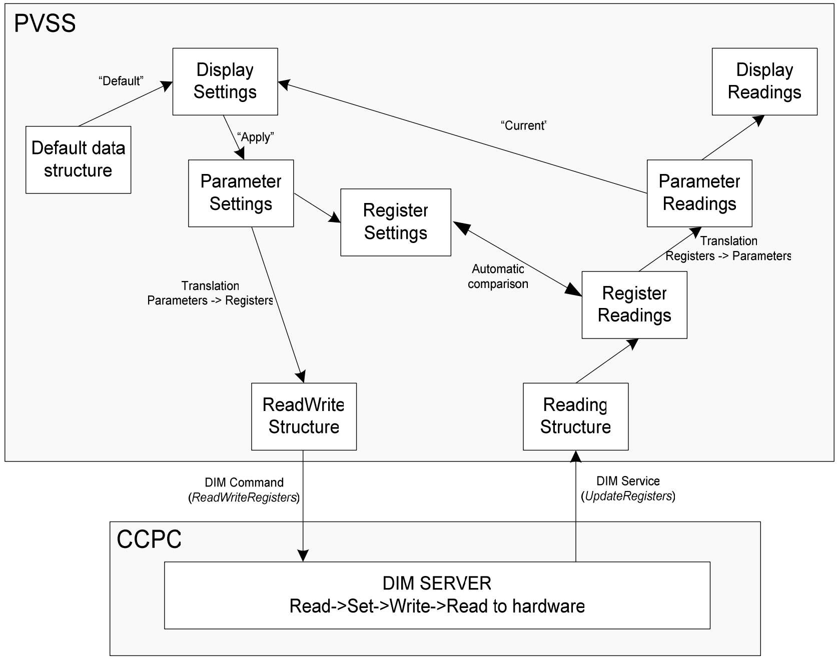
- Device description
  - Device types are described by PVSS data pint types
  - Similar for all device types
  - Each device is an instantiation of the data point type
- *State* is for the Finite State Machine (SMI) implementation
- *Registers* are physical board registers
- *Parameters* are functional variables
- Registers and parameters are stored as *Readings* and *Settings*
  - Automatic verification of write actions
- Parameters are organized in logical blocks
  - A parameters of a logical block are applied together
- Apply data point element
  - Allow calling functions which act on data point
- Actions
  - Data structures associated with the DIM commands and services



```
BoardType {
        int BoardID
        struct FPGAcode { string Q1
                        …}
        struct State {
                int RunState
                …}
        struct Registers {
                struct Readings {
                        struct Q1 { int R000
                                …}
                        struct I2C_40 { int R00
                                …}
                        …}
                struct Settings {
                        struct Q1 { int R000
                                …}
                        struct I2C_40 { int R00
                                …}
                        …}
        struct Parameters {
                struct Readings {
                        struct HW { int H_CLK_EXT
                                …}
                        struct Status { int S_ERR_PWR
                                …}
                        …}
                struct Settings {
                        struct HW { int H_CLK_EXT
                                …}
                        struct Status { int S_ERR_PWR
                                …}
                        …}
                int Apply }
        struct Actions {
                struct ReadWriteRegisters {}
                struct UpdateRegisters {}
                struct SubscribeRegisters {}
                struct UpdateSubscribedRegisters {}
                struct DownloadFPGA {}
                struct FPGALoadStatus {} }
        }
```

TFC Local Control System

- Flow chart of the register write access and subscription of status and counter data



PVSS

"Default"

Display Settings

Default data structure

"Apply"

Parameter Settings

Register Settings

"Current'

Display Readings

Parameter Readings

Translation Registers -> Parameters

Automatic comparison

Register Readings

Translation Parameters -> Registers

ReadWrite Structure

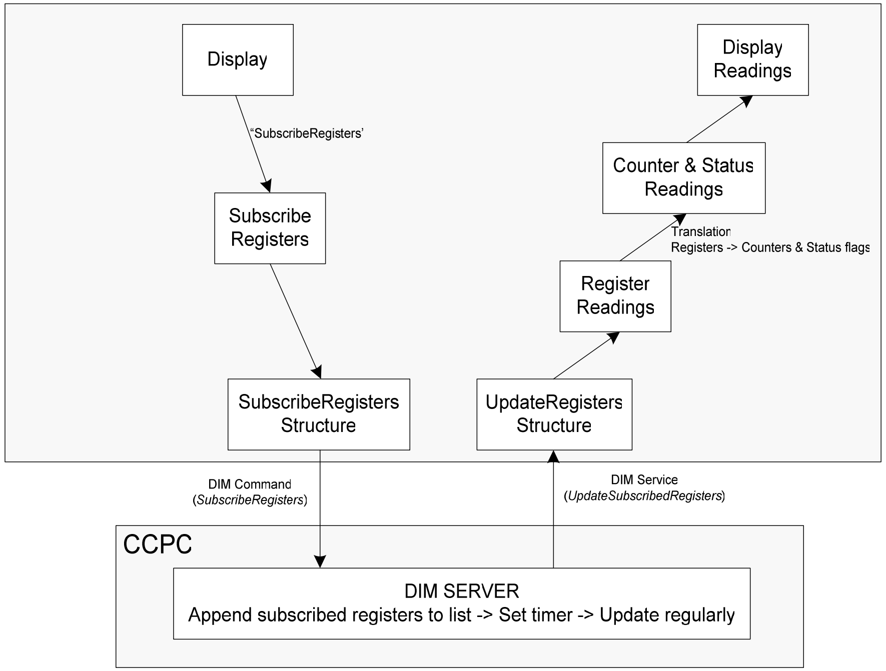
Reading Structure

DIM Command (*ReadWriteRegisters*)

DIM Service (*UpdateRegisters*)

CCPC

DIM SERVER
Read->Set->Write->Read to hardware



Display

Display Readings

'SubscribeRegisters'

Counter & Status Readings

Subscribe Registers

Translation Registers -> Counters & Status flags

Register Readings

SubscribeRegisters Structure

UpdateRegisters Structure

DIM Command (*SubscribeRegisters*)

DIM Service (*UpdateSubscribedRegisters*)

CCPC

DIM SERVER
Append subscribed registers to list -> Set timer -> Update regularly

TFC Control System

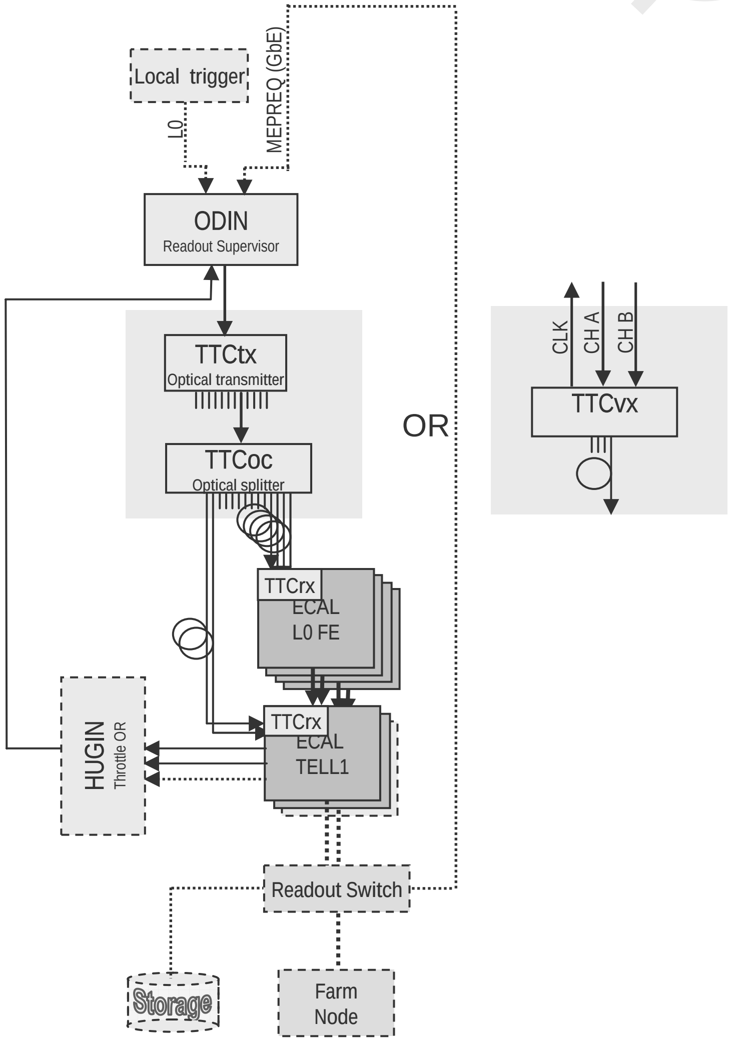
- Apply functions on for instance ODIN:
  - SystemReset(odin_name);
  - SoftReset(odin_name);
  - Initialize(odin_name);
  - ResetAllCounters(odin_name);
  - UpdateAllCounters(odin_name);
  - SubscribeAllCounters(odin_name);
  - UpdateAll(odin_name);
  - AckError(odin_name);
  - GetReady(odin_name);
  - RunStart(odin_name);
  - RunEnd(odin_name);
  - RunPause(odin_name);
  - RunContinue(odin_name);
  - GetHWinfo(odin_name);
  - Apply_HW_System(odin_name);
  - Apply_L0(odin_name);
  - Apply_Random(odin_name);
  - Apply_TriggerSM(odin_name);
  - DemandSingleTRG_A(odin_name);
  - etc

- Additional functions:
  - ODIN_GetParametersAll(string type);
  - ODIN_GetParametersL0(string type);
  - ODIN_GetParametersCommandSM(string type);
  - Etc
  - Where *type* is the name of a saved default

- All this together allows (will) scripting in PVSS entire automatic run sequences
  - Run as a single remote PVSS script without using GUI
  - Have to get recipe caching working

TFC Hardware Installation

- Throttle cable
- Single mode fibre
  - Order via TS/EL (Luit Koert de Jonge et al)
  - Type: CERN-ST/ST09S00*200* (2m)



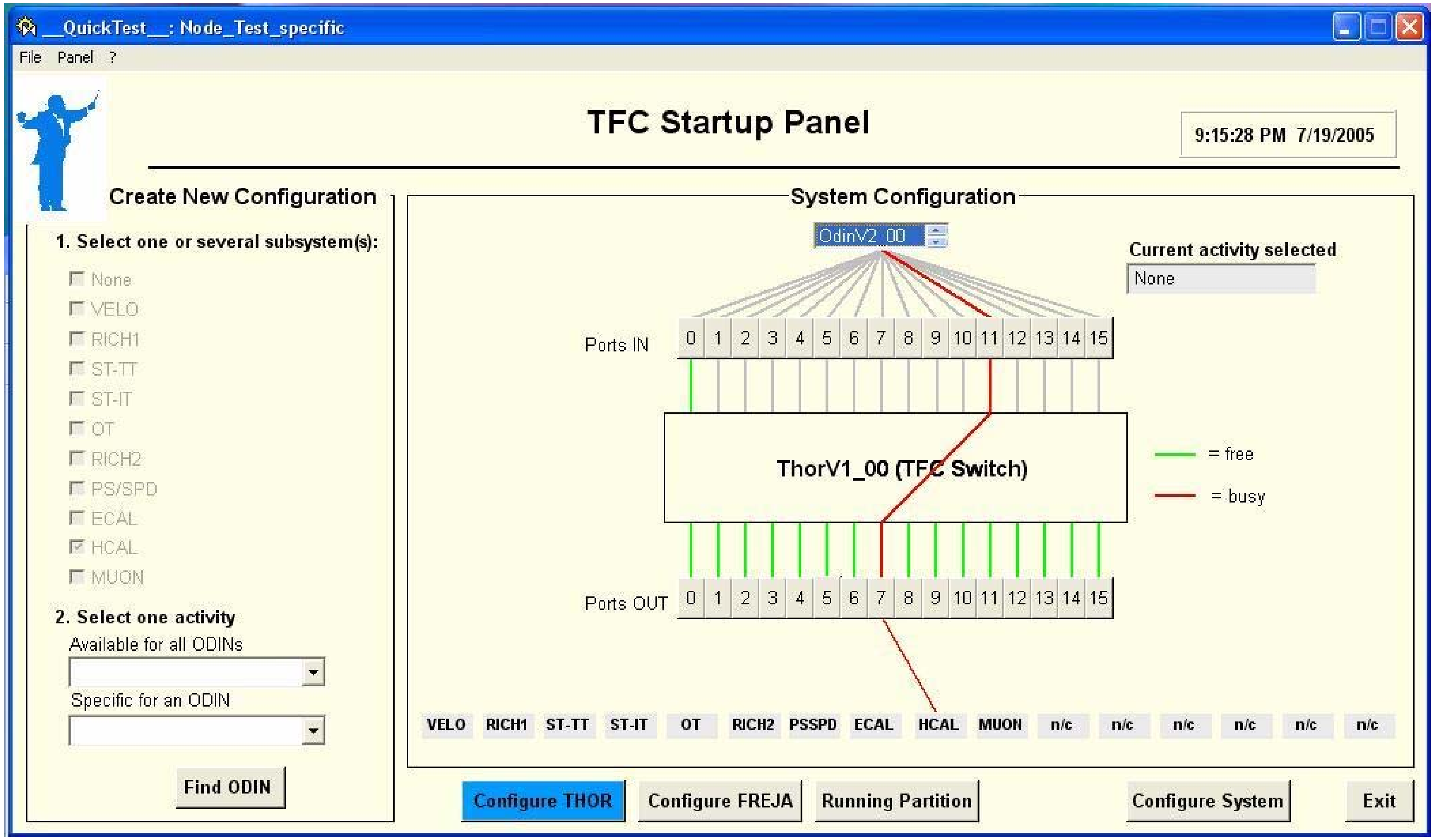
Starting Up

- Starting up
  1. Start up the DIM_DNS first
     1. Enter the directory ~/PVSS_tfc/framework_<date>/bin
     2. Start Dns.exe
  2. Start the PVSS project TFC_LC
  3. Login to the account ‘tfc’ on ODIN
     - Don’t modify anything on this account!
  4. Enter the directory ODIN_V1 or ODIN_V2 depending on the version
  5. Run the default setup file: > `source .setup_def`
  6. Start the TFC_server (TFC_server <DIM_DNS_NODE>)

- On Windows start entire PVSS project and GUI by:
  - Start PVSS Console from program menu and launch (I will set up script some time…)
  - Icon: C:\ETM\PVSS2\3.0\bin\PVSS00nv.exe -data <PVSS node> -event <PVSS node> -config C:\PCSS_tfc\TFC_LC\config\config –p TFC_top.pnl

- On Linux start entire PVSS project and GUI by:
  - PVSS00pmon –config /local_account/PVSS_tfc/TFC_LC/config/config &
  - PVSS00ui –config /local_accont/PVSS_tfc/TFC_LC/config/config –p TFC_top.pnl

Operating TFC_LC



__QuickTest__: Node_Test_specific

TFC Startup Panel

9:15:28 PM 7/19/2005

Create New Configuration

1. Select one or several subsystem(s):

- ☐ None
- ☐ VELO
- ☐ RICH1
- ☐ ST-TT
- ☐ ST-IT
- ☐ OT
- ☐ RICH2
- ☐ PS/SPD
- ☐ ECAL
- ☑ HCAL
- ☐ MUON

2. Select one activity

Available for all ODINs

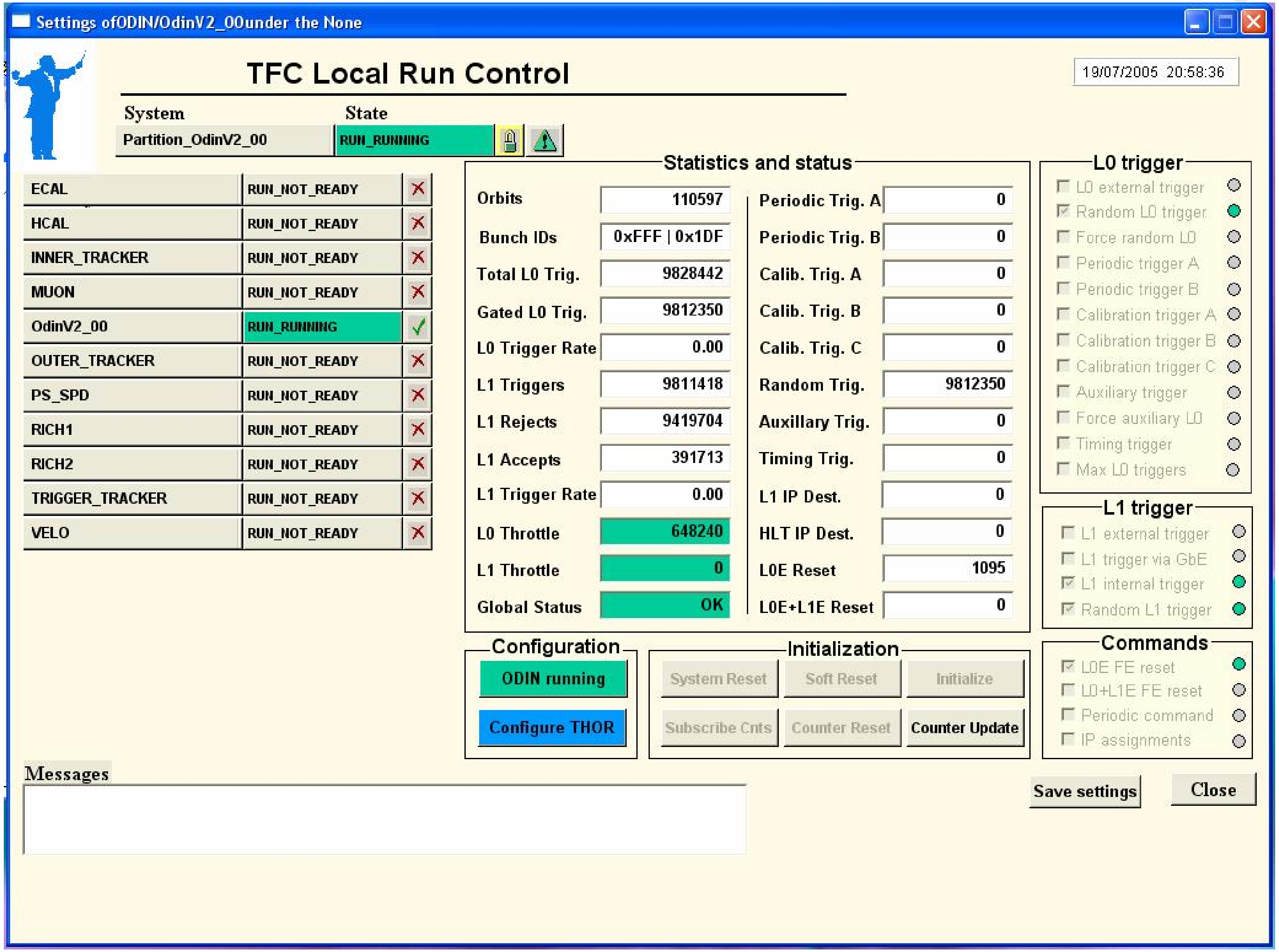
Specific for an ODIN

System Configuration

OdinV2_00

Current activity selected: None

Operating TFC_LC



Settings ofODIN/OdinV2_00under the None

TFC Local Run Control

19/07/2005 20:58:36

System	State
Partition_OdinV2_00	RUN_RUNNING

ECAL	RUN_NOT_READY	✗
HCAL	RUN_NOT_READY	✗
INNER_TRACKER	RUN_NOT_READY	✗
MUON	RUN_NOT_READY	✗
OdinV2_00	RUN_RUNNING	✓
OUTER_TRACKER	RUN_NOT_READY	✗
PS_SPD	RUN_NOT_READY	✗
RICH1	RUN_NOT_READY	✗
RICH2	RUN_NOT_READY	✗
TRIGGER_TRACKER	RUN_NOT_READY	✗
VELO	RUN_NOT_READY	✗

Statistics and status

Orbits	110597	Periodic Trig. A	0
Bunch IDs	0xFFF | 0x1DF	Periodic Trig. B	0
Total L0 Trig.	9828442	Calib. Trig. A	0
Gated L0 Trig.	9812350	Calib. Trig. B	0
L0 Trigger Rate	0.00	Calib. Trig. C	0
L1 Triggers	9811418	Random Trig.	9812350
L1 Rejects	9419704	Auxillary Trig.	0
L1 Accepts	391713	Timing Trig.	0
L1 Trigger Rate	0.00	L1 IP Dest.	0
L0 Throttle	648240	HLT IP Dest.	0
L1 Throttle	0	L0E Reset	1095
Global Status	OK	L0E+L1E Reset	0

L0 trigger

- ☐ L0 external trigger ○
- ☑ Random L0 trigger ●
- ☐ Force random L0 ○
- ☐ Periodic trigger A ○
- ☐ Periodic trigger B ○
- ☐ Calibration trigger A ○
- ☐ Calibration trigger B ○
- ☐ Calibration trigger C ○
- ☐ Auxiliary trigger ○
- ☐ Force auxiliary L0 ○
- ☐ Timing trigger ○
- ☐ Max L0 triggers ○

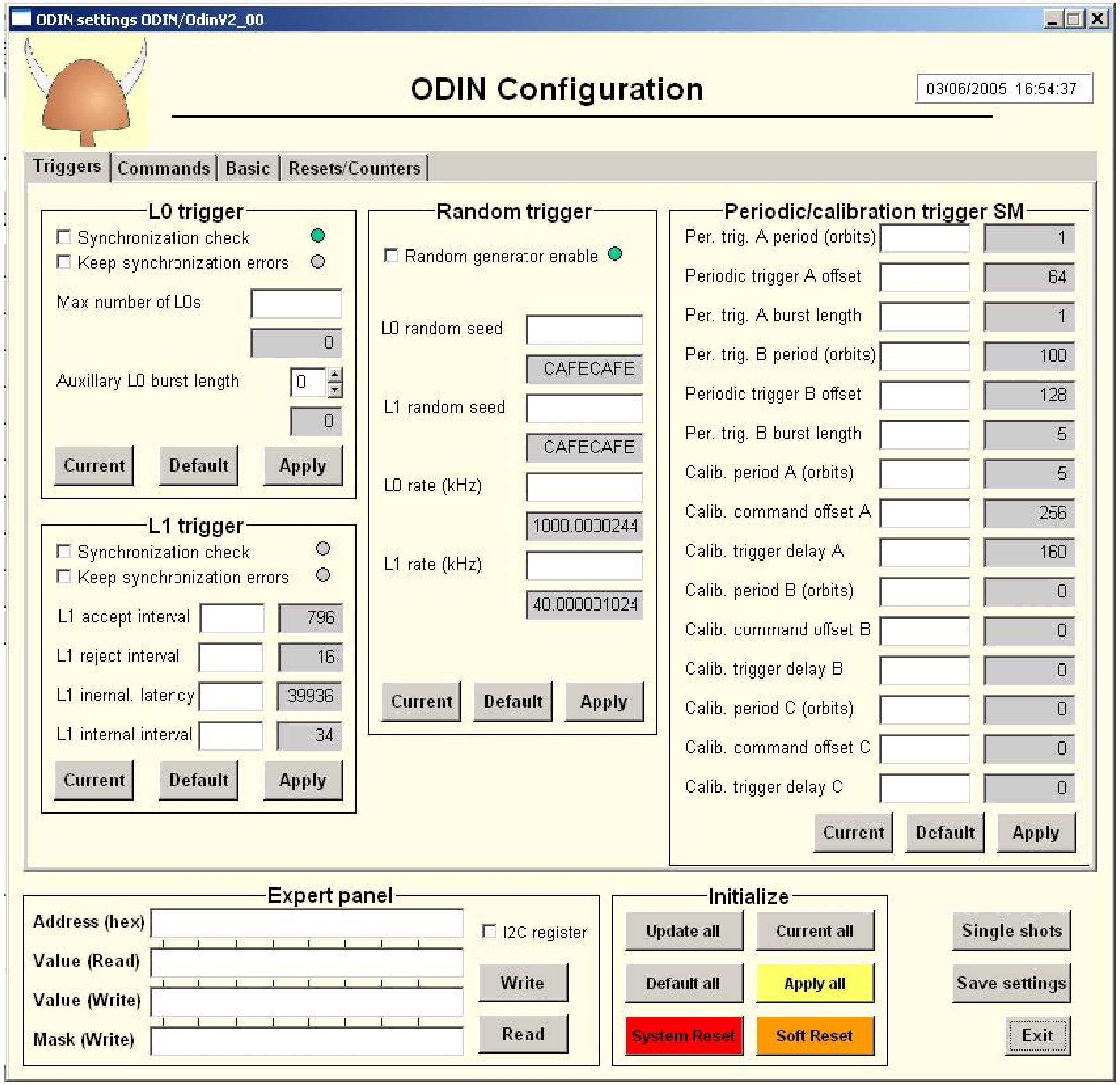
L1 trigger

- ☐ L1 external trigger ○
- ☐ L1 trigger via GbE ○
- ☑ L1 internal trigger ●
- ☑ Random L1 trigger ●

Commands

- ☑ L0E FE reset ●
- ☐ L0+L1E FE reset ○
- ☐ Periodic command ○
- ☐ IP assignments ○

Operating TFC_LC



ODIN settings ODIN/OdinV2_00

ODIN Configuration

03/06/2005 16:54:37

Triggers | Commands | Basic | Resets/Counters

L0 trigger

- □ Synchronization check ●
- □ Keep synchronization errors ○

Max number of L0s: 0

Auxillary L0 burst length: 0 / 0

L1 trigger

- □ Synchronization check ○
- □ Keep synchronization errors ○

L1 accept interval	796
L1 reject interval	16
L1 inernal. latency	39936
L1 internal interval	34

Random trigger

- □ Random generator enable ●

L0 random seed	CAFECAFE
L1 random seed	CAFECAFE
L0 rate (kHz)	1000.0000244
L1 rate (kHz)	40.000001024

Periodic/calibration trigger SM

Per. trig. A period (orbits)	1
Periodic trigger A offset	64
Per. trig. A burst length	1
Per. trig. B period (orbits)	100
Periodic trigger B offset	128
Per. trig. B burst length	5
Calib. period A (orbits)	5
Calib. command offset A	256
Calib. trigger delay A	160
Calib. period B (orbits)	0
Calib. command offset B	0
Calib. trigger delay B	0
Calib. period C (orbits)	0
Calib. command offset C	0
Calib. trigger delay C	0

Expert panel

Address (hex)

Value (Read)

Value (Write)

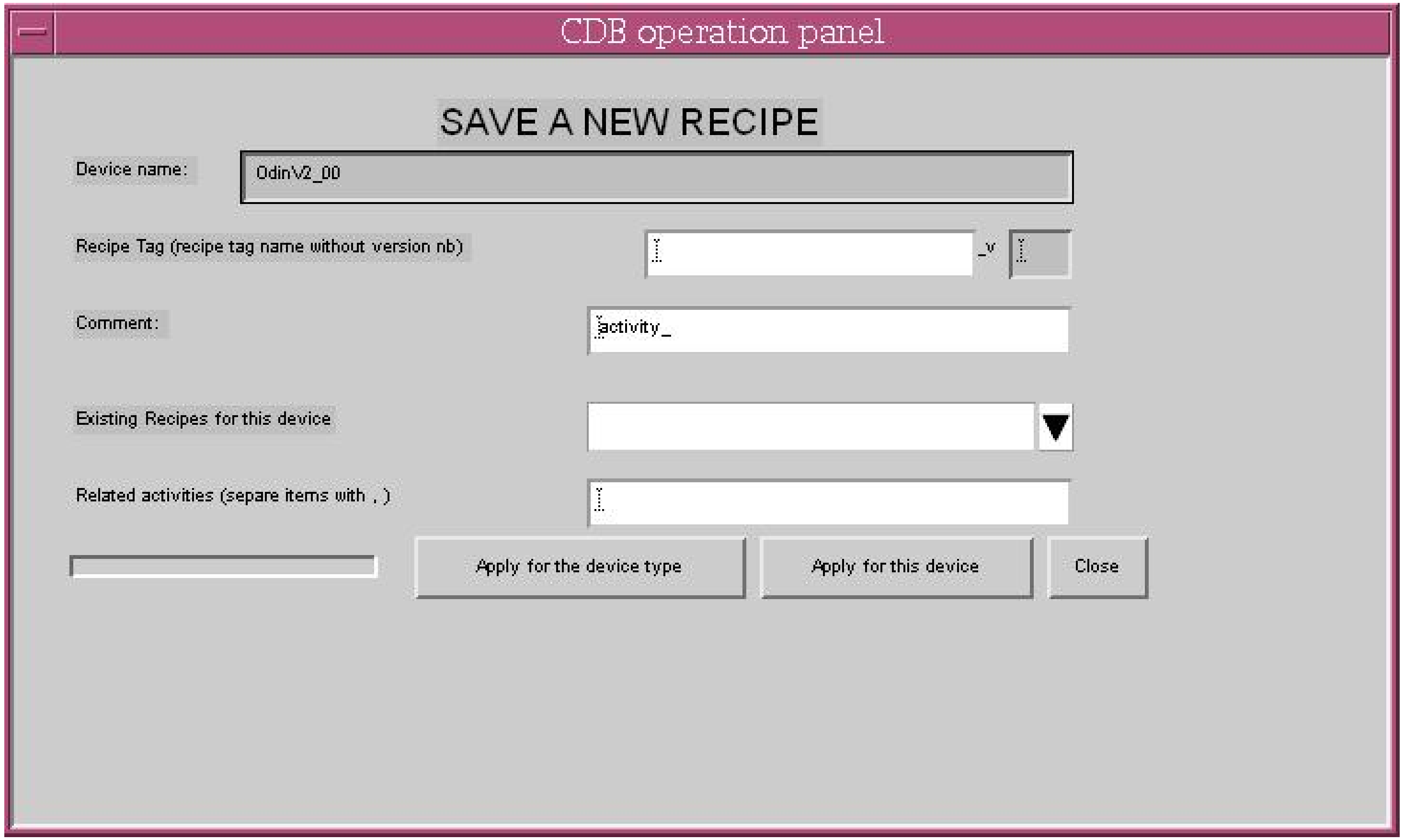
Mask (Write)

□ I2C register

Initialize

Operating TFC_LC

- Recipes



CDB operation panel

SAVE A NEW RECIPE

Device name: OdinV2_00

Recipe Tag (recipe tag name without version nb) _v

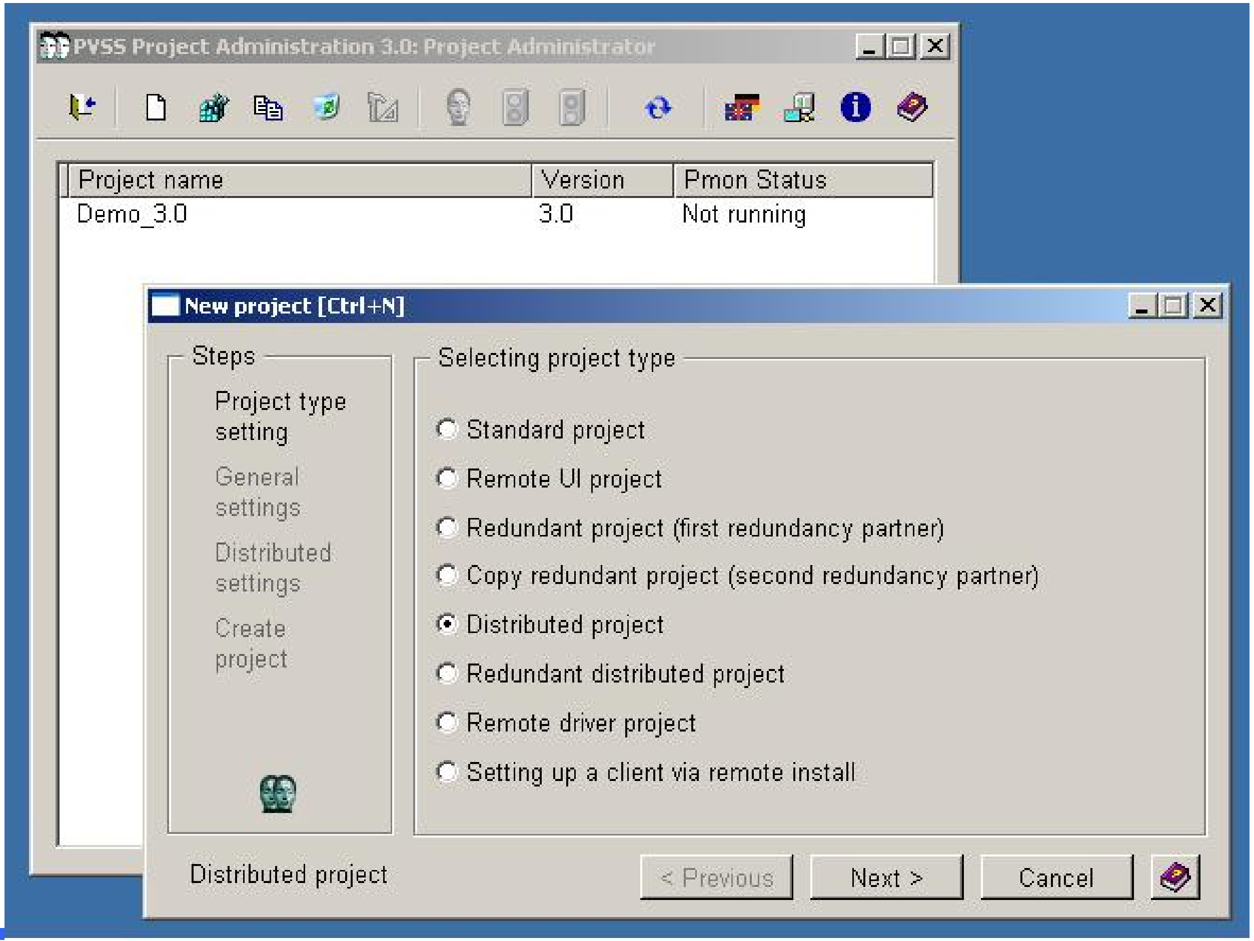
Comment: activity_

Existing Recipes for this device

Related activities (separe items with ,)

TFC_LC Installation 1

- Attention 1: Use versions of JCOP framework components as stated in installation document in TFC_LC distribution
- Attention 2: On Linux, unzip –a <file.zip>
- First, create new PVSS project



Project name	Version	Pmon Status
Demo_3.0	3.0	Not running

Steps

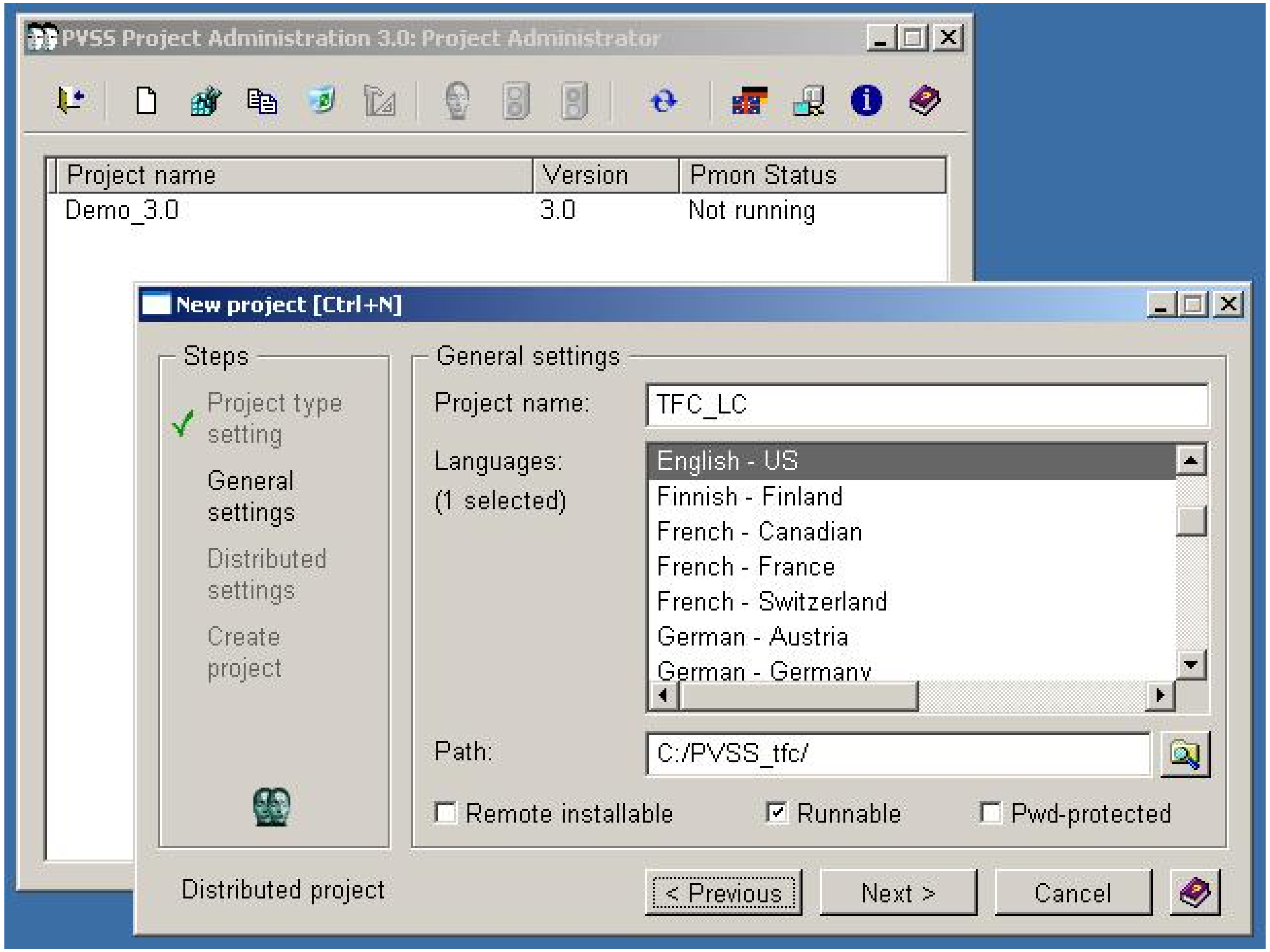
- Project type setting
- General settings
- Distributed settings
- Create project

Selecting project type

○ Standard project
○ Remote UI project
○ Redundant project (first redundancy partner)
○ Copy redundant project (second redundancy partner)
● Distributed project
○ Redundant distributed project
○ Remote driver project
○ Setting up a client via remote install

Distributed project

TFC_LC Installation 2



PVSS Project Administration 3.0: Project Administrator

Project name	Version	Pmon Status
Demo_3.0	3.0	Not running

New project [Ctrl+N]

Steps

- ✓ Project type setting
- General settings
- Distributed settings
- Create project

General settings

Project name: TFC_LC

Languages: (1 selected)

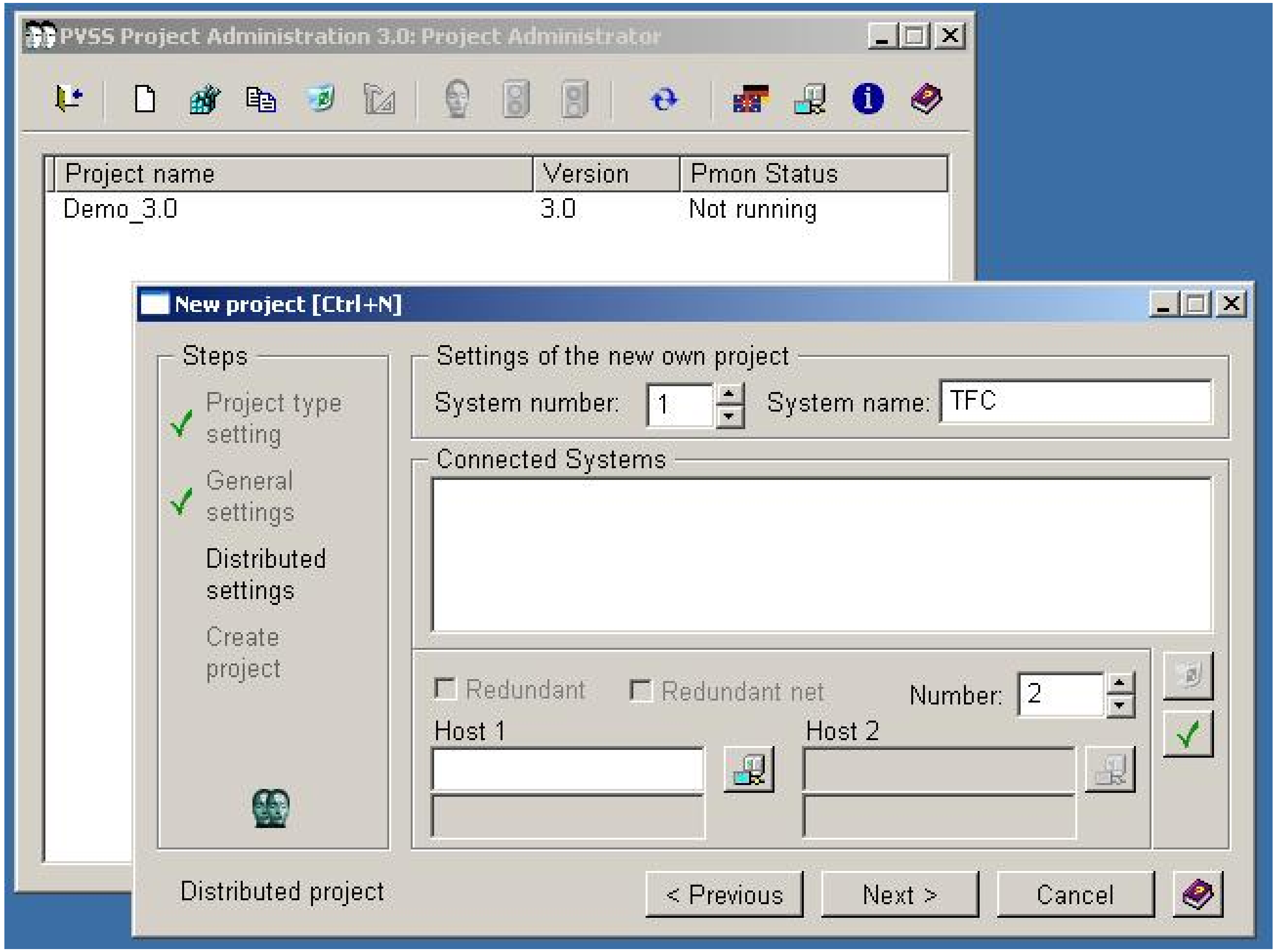
- English - US
- Finnish - Finland
- French - Canadian
- French - France
- French - Switzerland
- German - Austria
- German - Germany

Path: C:/PVSS_tfc/

□ Remote installable ☑ Runnable □ Pwd-protected

Distributed project

TFC_LC Installation 3



PVSS Project Administration 3.0: Project Administrator

Project name	Version	Pmon Status
Demo_3.0	3.0	Not running

New project [Ctrl+N]

Steps
- ✓ Project type setting
- ✓ General settings
- Distributed settings
- Create project

Settings of the new own project

System number: 1

System name: TFC

Connected Systems

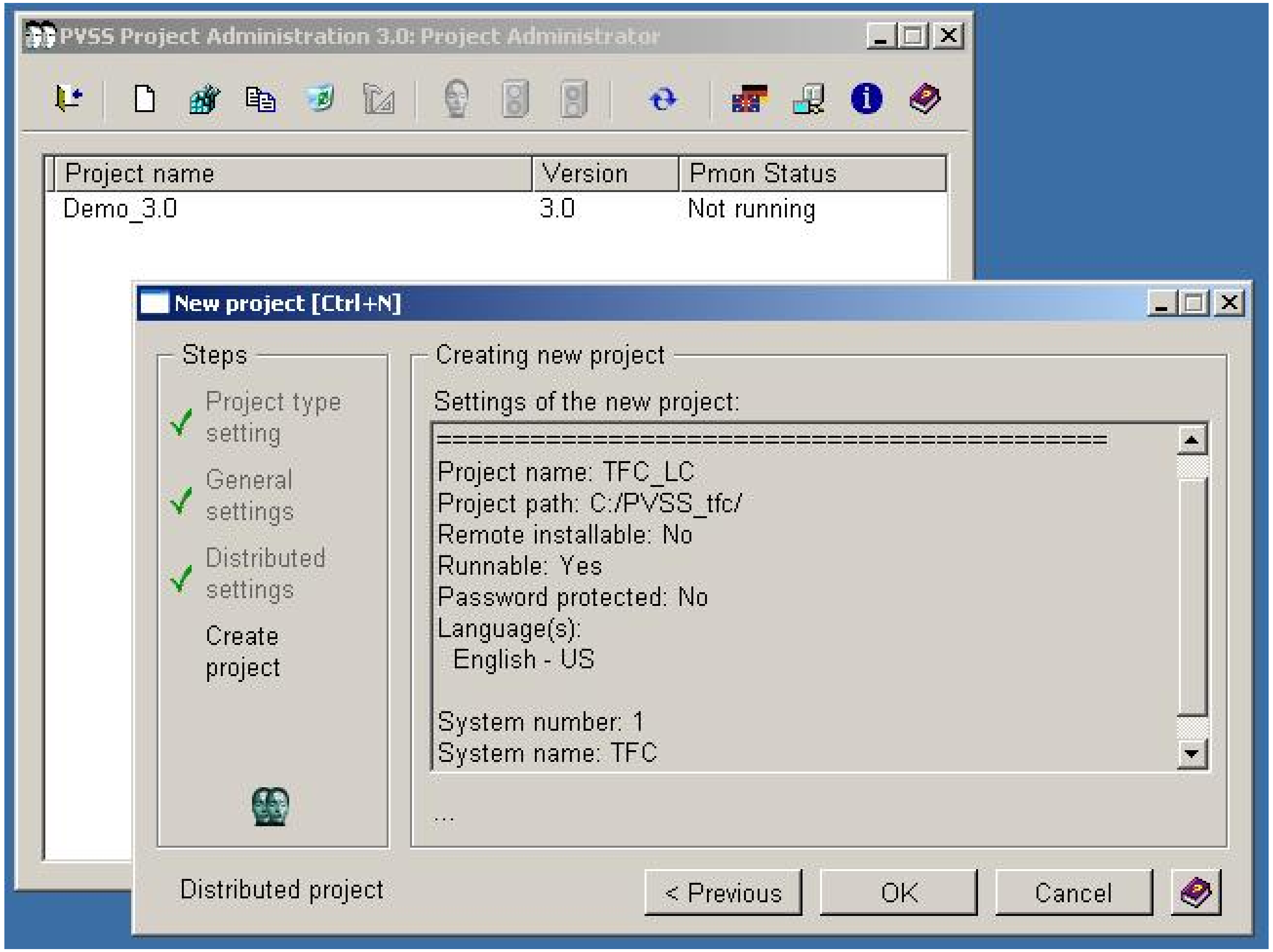
□ Redundant □ Redundant net Number: 2

Host 1

Host 2

Distributed project

TFC_LC Installation 4



Project name	Version	Pmon Status
Demo_3.0	3.0	Not running

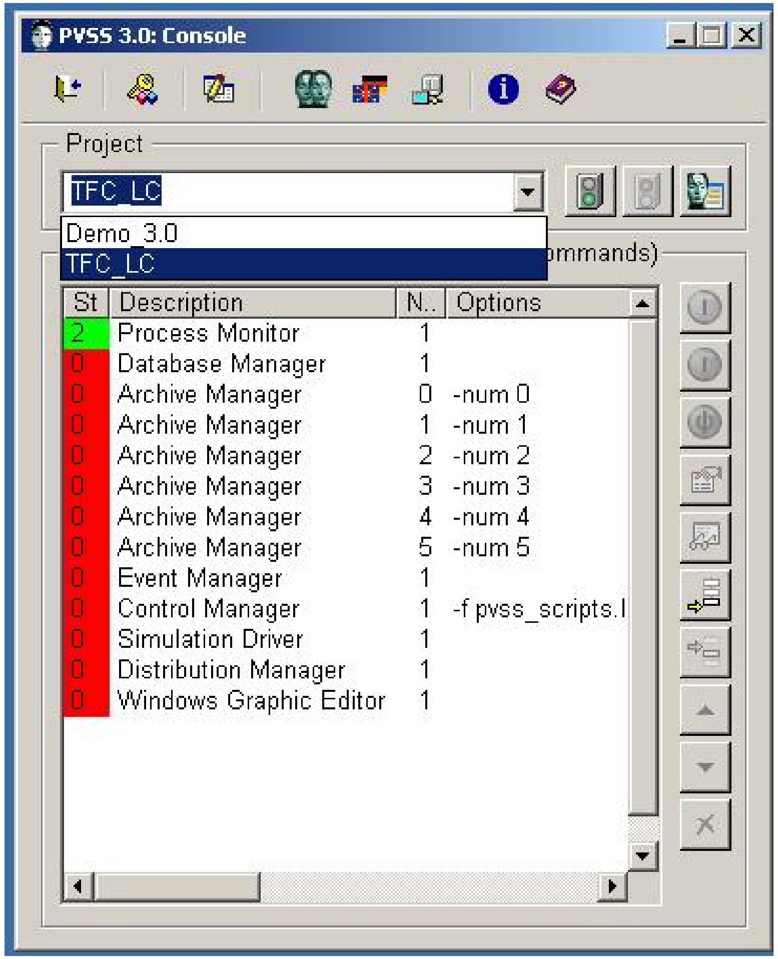
Settings of the new project:

```
==============================================
Project name: TFC_LC
Project path: C:/PVSS_tfc/
Remote installable: No
Runnable: Yes
Password protected: No
Language(s):
  English - US

System number: 1
System name: TFC
```

TFC_LC Installation 5

- Install fwInstallation tool before starting project
  - Instructions and download on http://itcobe.web.cern.ch/itcobe/Projects/Framework/Download/welcome.html



PVSS 3.0: Console

Project

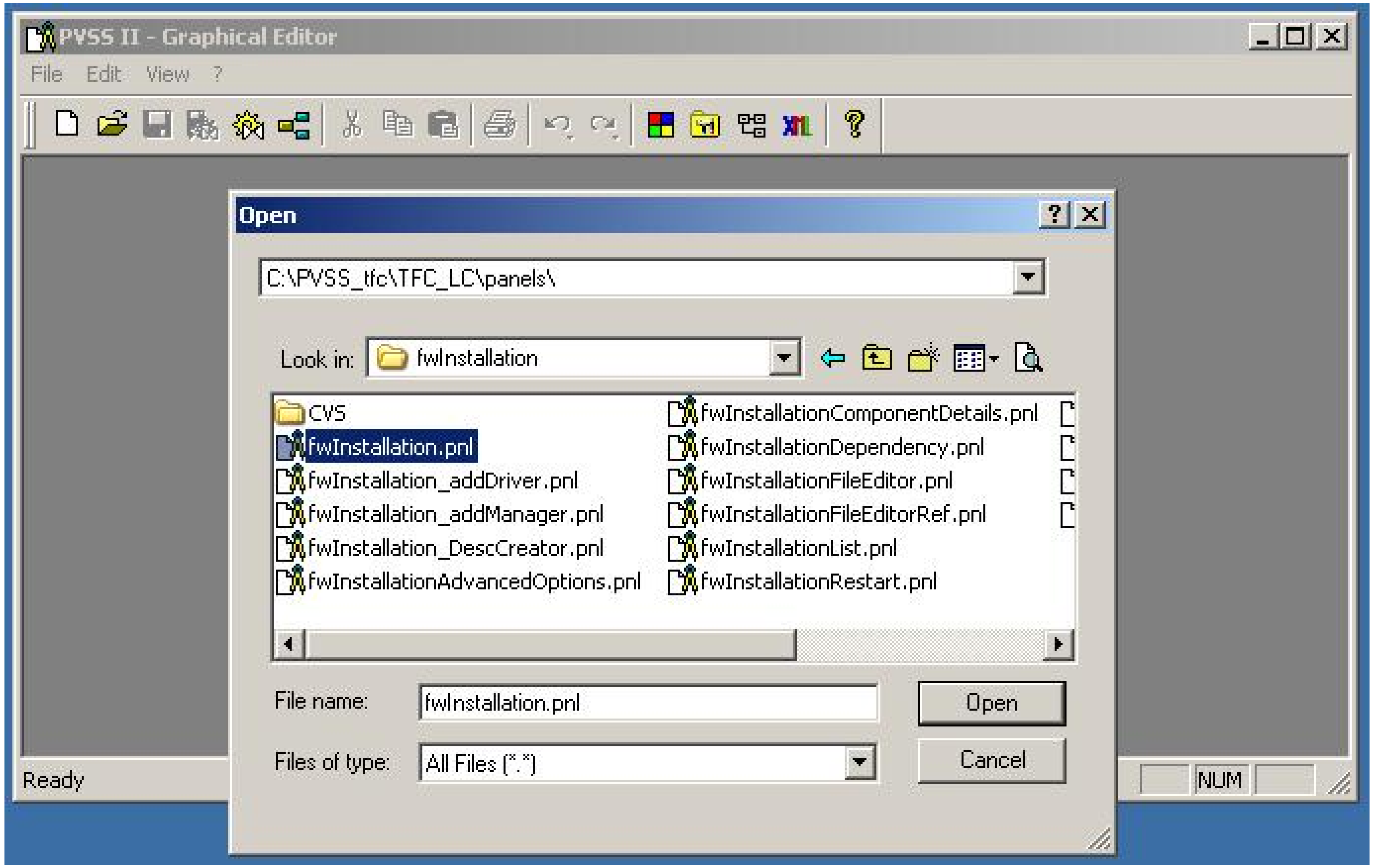
TFC_LC

Demo_3.0

TFC_LC

St	Description	N..	Options
2	Process Monitor	1	
0	Database Manager	1	
0	Archive Manager	0	-num 0
0	Archive Manager	1	-num 1
0	Archive Manager	2	-num 2
0	Archive Manager	3	-num 3
0	Archive Manager	4	-num 4
0	Archive Manager	5	-num 5
0	Event Manager	1	
0	Control Manager	1	-f pvss_scripts.l
0	Simulation Driver	1	
0	Distribution Manager	1	
0	Windows Graphic Editor	1	

TFC_LC Installation 6



PVSS II - Graphical Editor

Open

C:\PVSS_tfc\TFC_LC\panels\

Look in: fwInstallation

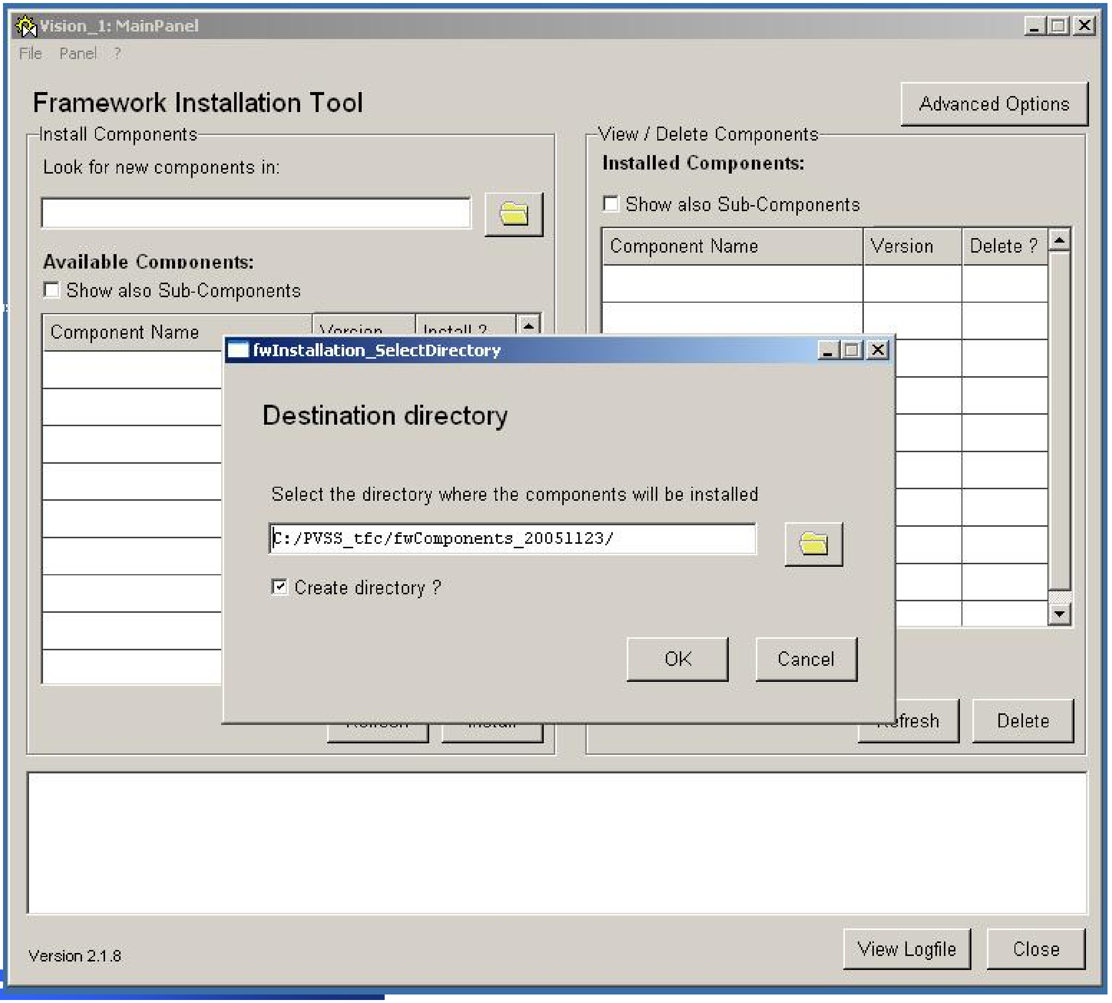
- CVS
- fwInstallation.pnl
- fwInstallation_addDriver.pnl
- fwInstallation_addManager.pnl
- fwInstallation_DescCreator.pnl
- fwInstallationAdvancedOptions.pnl
- fwInstallationComponentDetails.pnl
- fwInstallationDependency.pnl
- fwInstallationFileEditor.pnl
- fwInstallationFileEditorRef.pnl
- fwInstallationList.pnl
- fwInstallationRestart.pnl

File name: fwInstallation.pnl

Files of type: All Files (*.*)

TFC_LC Installation 7

- Install JCOP framework components fwConfigurationDB, fwCore, fwDIM
  - Instructions and download on: http://itcobe.web.cern.ch/itcobe/Projects/Framework/Download/welcome.html



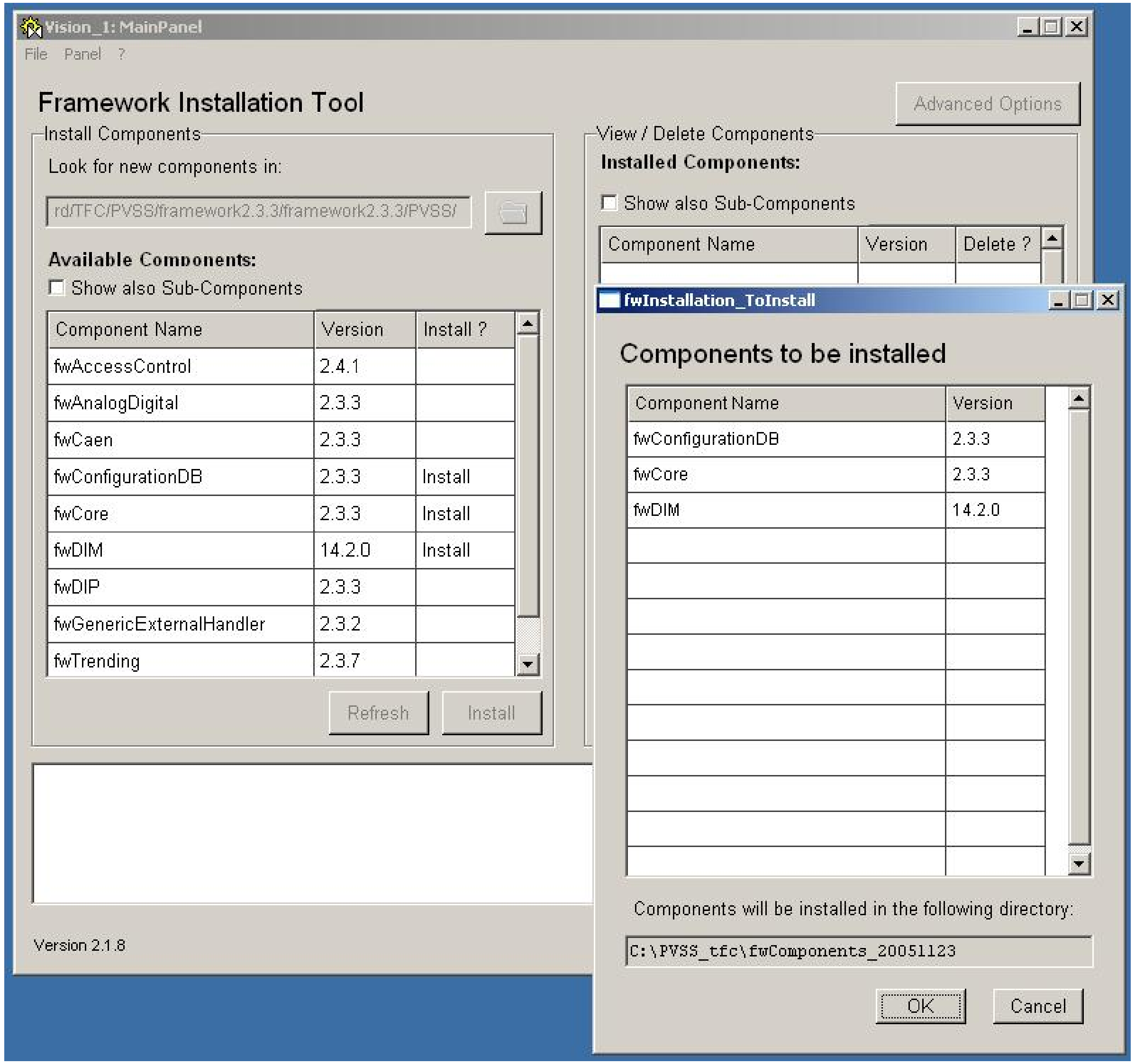
Destination directory

Select the directory where the components will be installed

C:/PVSS_tfc/fwComponents_20051123/

☑ Create directory ?

TFC_LC Installation 8



Framework Installation Tool

Install Components

Look for new components in:

rd/TFC/PVSS/framework2.3.3/framework2.3.3/PVSS/

Available Components:

□ Show also Sub-Components

Component Name	Version	Install ?
fwAccessControl	2.4.1	
fwAnalogDigital	2.3.3	
fwCaen	2.3.3	
fwConfigurationDB	2.3.3	Install
fwCore	2.3.3	Install
fwDIM	14.2.0	Install
fwDIP	2.3.3	
fwGenericExternalHandler	2.3.2	
fwTrending	2.3.7	

View / Delete Components

Installed Components:

□ Show also Sub-Components

Component Name	Version	Delete ?

Version 2.1.8

fwInstallation_ToInstall

Components to be installed

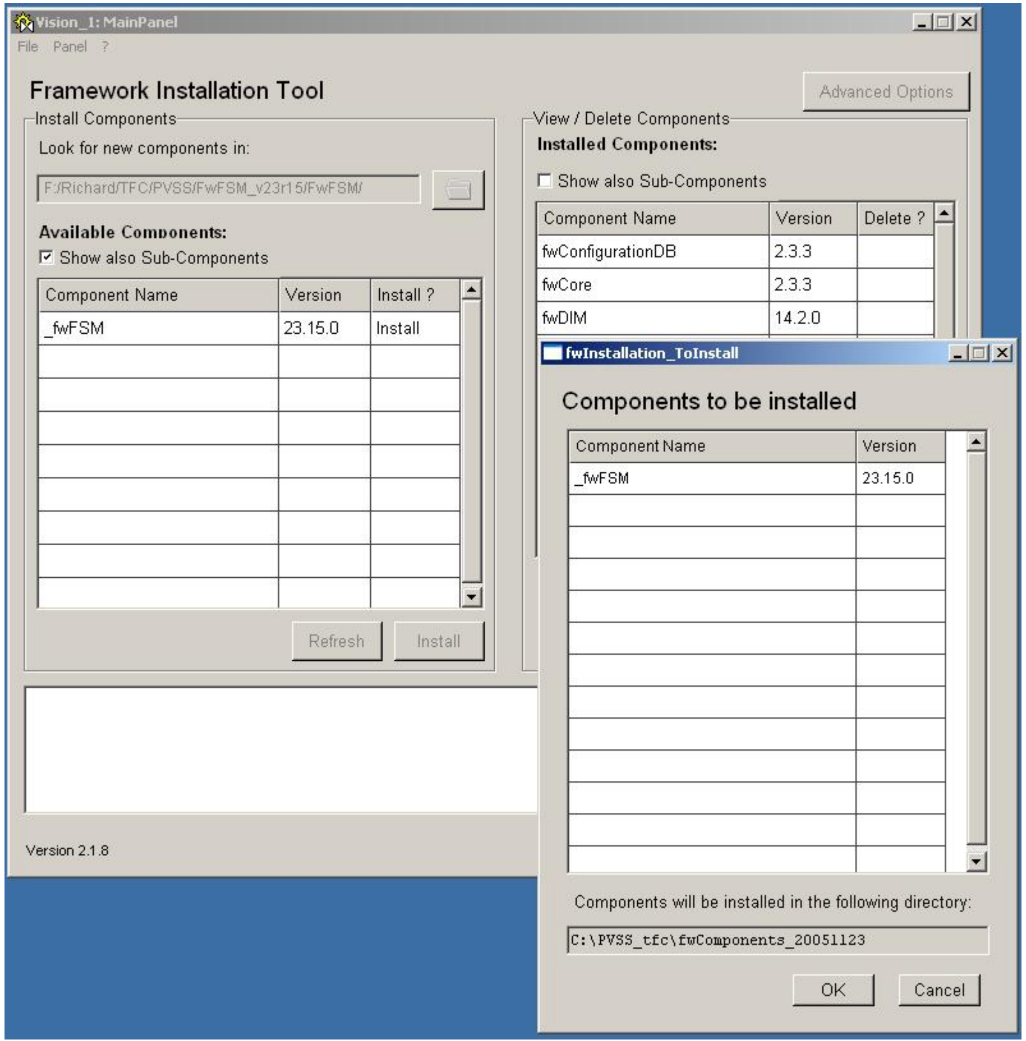
Component Name	Version
fwConfigurationDB	2.3.3
fwCore	2.3.3
fwDIM	14.2.0

Components will be installed in the following directory:

C:\PVSS_tfc\fwComponents_20051123

TFC_LC Installation 9

- Install framework component fwFSM (If latest TFC installation instructions says so…)
  - Download the framework component from http://clara.home.cern.ch/clara/fw/FW_FSM.HTML



Framework Installation Tool

Install Components

Look for new components in:

F:/Richard/TFC/PVSS/FwFSM_v23r15/FwFSM/

Available Components:

☑ Show also Sub-Components

Component Name	Version	Install ?
_fwFSM	23.15.0	Install

Version 2.1.8

View / Delete Components

Installed Components:

□ Show also Sub-Components

Component Name	Version	Delete ?
fwConfigurationDB	2.3.3	
fwCore	2.3.3	
fwDIM	14.2.0	

Components to be installed

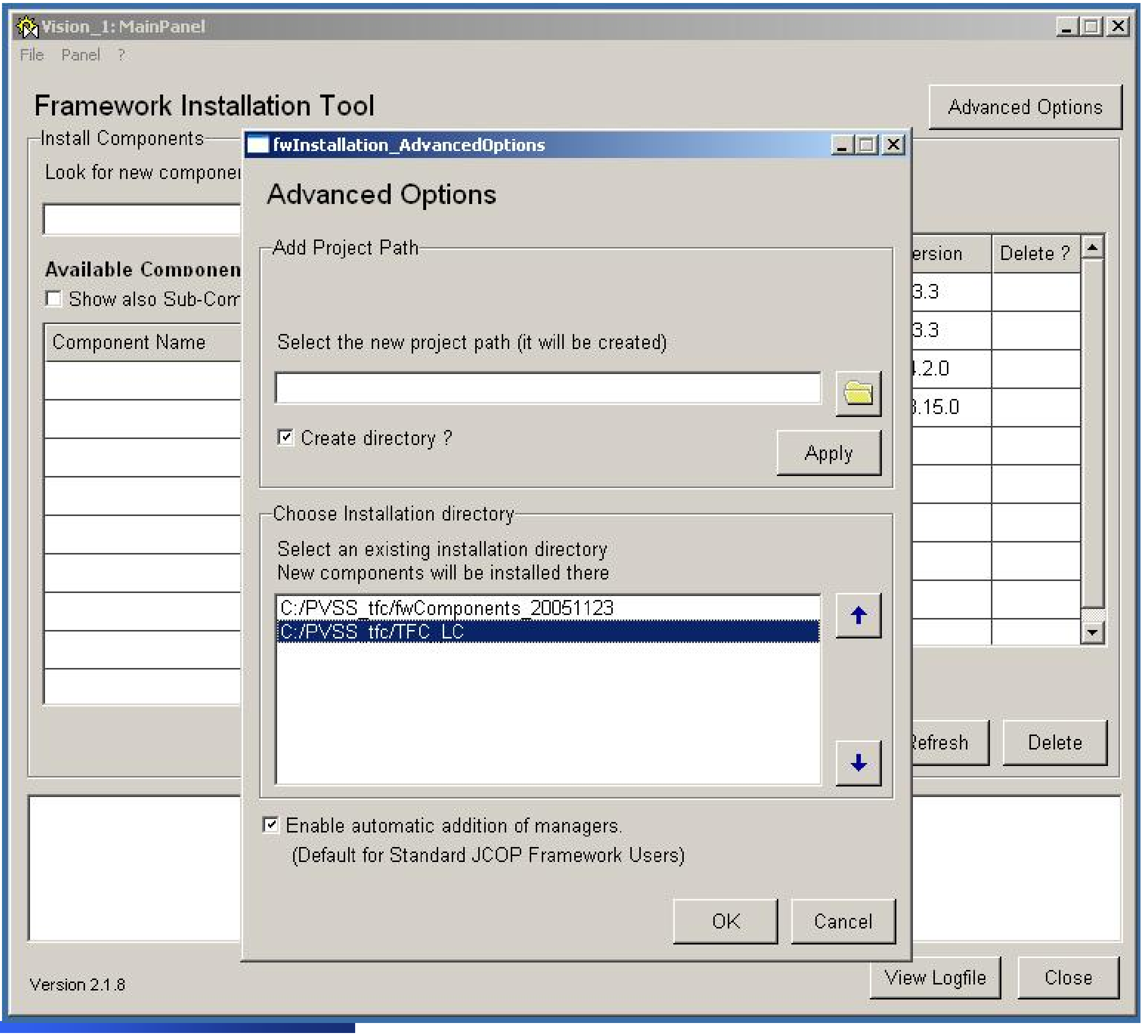
Component Name	Version
_fwFSM	23.15.0

Components will be installed in the following directory:

C:\PVSS_tfc\fwComponents_20051123

TFC_LC Installation 10

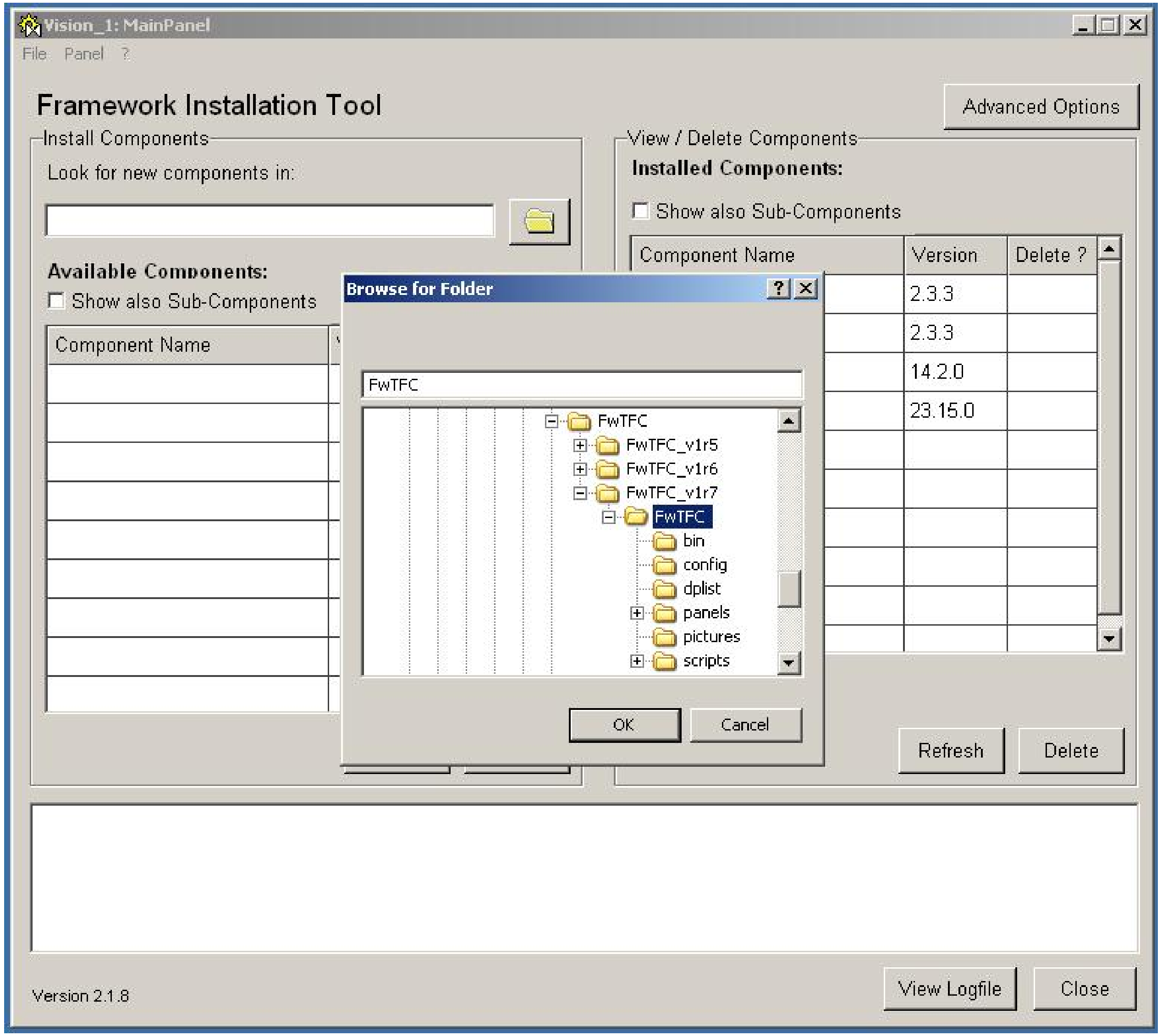
1. Get the TFC_LC framework component (current version 1.7)
2. Change DIM_DNS_NODE in ~/FwTFC<version>/config/FwTFC.postInstall
3. Install TFC_LC framework component



Vision_1: MainPanel
File Panel ?
Framework Installation Tool
Advanced Options
Install Components
Look for new componer
Available Componen
□ Show also Sub-Com
Component Name
ersion
Delete ?
3.3
3.3
.2.0
.15.0
efresh
Delete
Version 2.1.8
View Logfile
Close
fwInstallation_AdvancedOptions
Advanced Options
Add Project Path
Select the new project path (it will be created)
☑ Create directory ?
Apply
Choose Installation directory
Select an existing installation directory
New components will be installed there
☑ Enable automatic addition of managers.
(Default for Standard JCOP Framework Users)
OK
Cancel

C:/PVSS_tfc/fwComponents_20051123
C:/PVSS_tfc/TFC_LC

TFC_LC Installation 11



Vision_1: MainPanel

File Panel ?

Framework Installation Tool

Advanced Options

Install Components

Look for new components in:

Available Components:

□ Show also Sub-Components

Component Name

View / Delete Components

Installed Components:

□ Show also Sub-Components

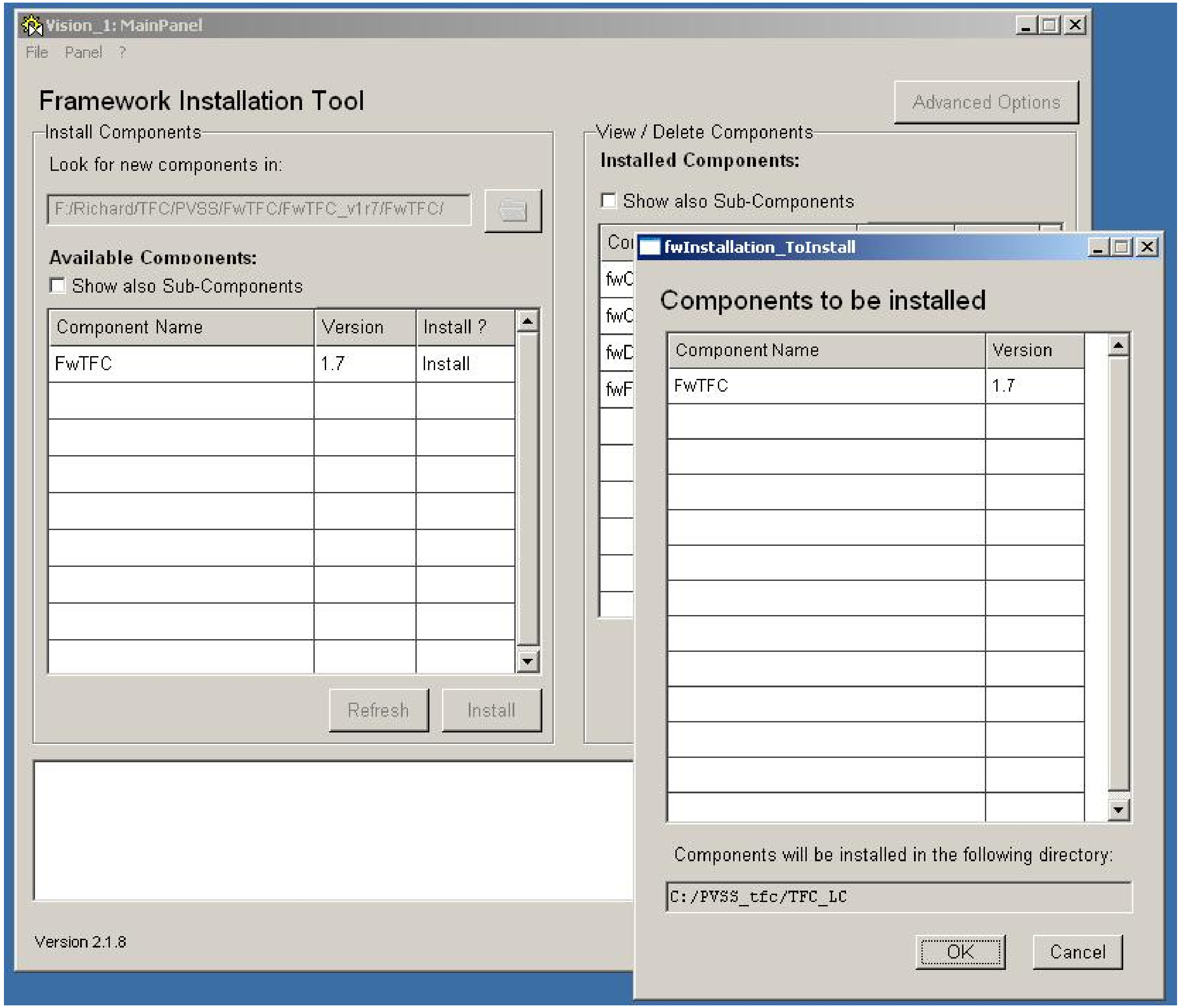
Component Name	Version	Delete ?
	2.3.3	
	2.3.3	
	14.2.0	
	23.15.0	

Browse for Folder

FwTFC

Version 2.1.8

TFC_LC Installation 12



Framework Installation Tool

Install Components

Look for new components in: F:/Richard/TFC/PVSS/FwTFC/FwTFC_v1r7/FwTFC/

Available Components:

□ Show also Sub-Components

Component Name	Version	Install ?
FwTFC	1.7	Install

View / Delete Components

Installed Components:

□ Show also Sub-Components

Version 2.1.8

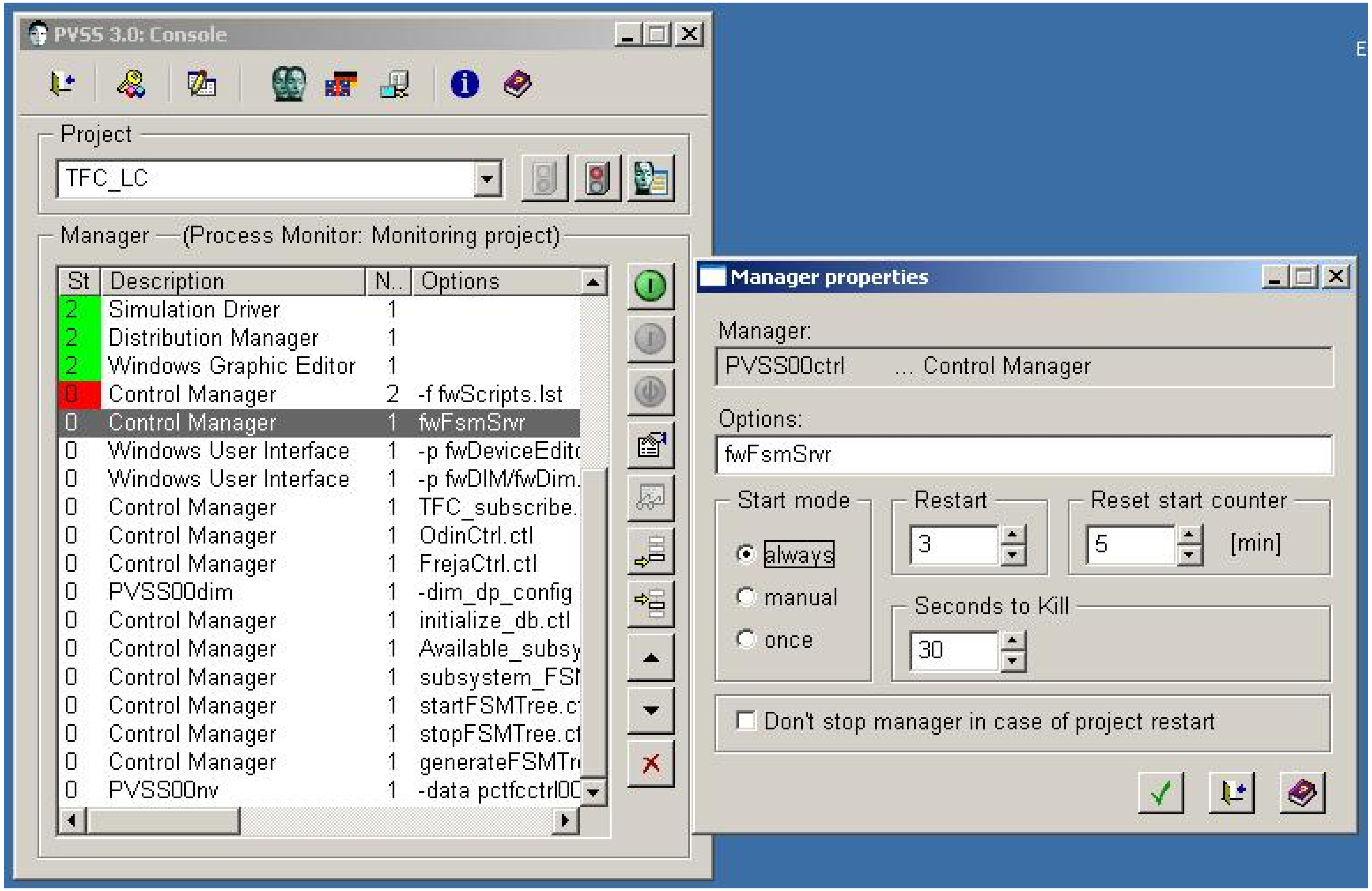
Components to be installed

Component Name	Version
FwTFC	1.7

Components will be installed in the following directory:

```
C:/PVSS_tfc/TFC_LC
```

TFC_LC Installation 13



PVSS 3.0: Console

Project: TFC_LC

Manager —(Process Monitor: Monitoring project)

St	Description	N..	Options
2	Simulation Driver	1	
2	Distribution Manager	1	
2	Windows Graphic Editor	1	
0	Control Manager	2	-f fwScripts.lst
0	Control Manager	1	fwFsmSrvr
0	Windows User Interface	1	-p fwDeviceEdit
0	Windows User Interface	1	-p fwDIM/fwDim.
0	Control Manager	1	TFC_subscribe.
0	Control Manager	1	OdinCtrl.ctl
0	Control Manager	1	FrejaCtrl.ctl
0	PVSS00dim	1	-dim_dp_config
0	Control Manager	1	initialize_db.ctl
0	Control Manager	1	Available_subsy
0	Control Manager	1	subsystem_FSI
0	Control Manager	1	startFSMTree.c
0	Control Manager	1	stopFSMTree.ct
0	Control Manager	1	generateFSMTr
0	PVSS00nv	1	-data pctfcctrl0C

Manager properties

Manager: PVSS00ctrl ... Control Manager

Options: fwFsmSrvr

Start mode: ● always ○ manual ○ once

Restart: 3

Reset start counter: 5 [min]

Seconds to Kill: 30

□ Don't stop manager in case of project restart

TFC_LC Installation 14

- Change the run mode of the following PVSS managers :
  - "Control manager FwFsmSrv" - set to run "always"
  - "Control manager TFC_Subscribe.ctl" - set to run "once"
  - "Control manager OdinCtrl.ctl" - set to run "always"
  - Control manager ThorCtrl.ctl" - set to run “manual“
  - Control manager MuninCtrl.ctl" - set to run “manual“
  - Control manager HuginCtrl.ctl" - set to run "always“ if needed
  - "PVSS00DIM ...." - set to run "always"
  - "Control manager initialize_db.ctl" - set to run "once"
  - "Control manager Available_subsystems.ctl - set to run "once"
  - "Control manager subsystem_FSM.ctl" - set to run "always"
  - "Control manager startFSMTree.ctl" - set to run "once"

Getting equipment

- Currently we have 10 ODINs, two of which have developed a fault
  - Series of 18 ODINs will arrive at CERN week 49

- Current usage:

TFC @ CERN	OdinV2_00
ST @ Zurich	OdinV1_00
OT @ CERN	OdinV1_01
RICH @ Oxford	OdinV2_01
VELO @ CERN	OdinV2_02

- Cost of an ODIN: 4900 CHF

Documentation

- ODIN Technical Reference
  - Currently version describes ODIN with a L1 trigger…
- TFC mailing list
  - LHCb-TFC
  - Already added a number of you:
    - Marco Adinolfi - PH/ULB <Marco.Adinolfi@cern.ch>
      Jan Buytaert - PH/ED <Jan.Buytaert@cern.ch>
      Jorgen Christiansen - PH/ED <Jorgen.Christiansen@cern.ch>
      Pierre-Yves Duval - PH/ULB <duval@cppm.in2p3.fr>
      Lars Eklund - PH/LBD <Lars.Eklund@cern.ch>
      Guido Haefeli - PH/ULB <guido.haefeli@epfl.ch>
      Adriano Lai - PH/ULB <adriano.lai@ca.infn.it>
      Pascal Perret - PH/ULB <Pascal.Perret@cern.ch>
      Stig Topp-Jorgensen - PH/ULB <s.topp-jorgensen@physics.ox.ac.uk>
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- TFC Web is being remade
  - Will have all EDMS links to documents
  - Software downloads and instructions
- All is [going] in EDMS