DIGITAL-LOGIC
smart embedded computers

TECHNICAL USER'S MANUAL FOR:

smartModule

SM586PC

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REVISION HISTORY:

Prod.-Serialnumber: From: To:	Product Version	BIOS Version	Doc. Version	Date/Vis:	Modification: Remarks, News, Attention:
			V0.9	***01.2001 KUF***	***Initial Version***
	V1.3		V1.0	10.2001 KUF	Revised Version, Preliminary

PRODUCT REGISTRATION:

Please register your product under:

http://www.digitallogic.com -> SUPPORT -> Product Registration

After registration, you will receive driver & software updates, errata information, customer information and news from DIGITAL-LOGIC AG products automatically.

Table of Contents

1 PREFACE

This manual is for integrators and programmers of systems based on the smartModule-586PC system on chip family. It contains information on hardware requirements, interconnections, and details of how to program the system. The specifications given in this manual were correct at the time of printing; advances mean that some may have changed in the meantime.

1.1 How to use this manual

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the system on chip units. It provides instructions for designing, installing and configuring the unit, and describes the system and setup requirements.

1.2 Trademarks

Chips & Technologies	SuperState R
MICROSPACE, MicroModule	DIGITAL-LOGIC AG
DOS Vx.y, Windows	Microsoft Inc.
PC-AT, PC-XT	IBM
NetWare	Novell Corporation
Ethernet	Xerox Corporation
DR-DOS, PALMDOS	Digital Research Inc. / Novell Inc.
ROM-DOS	Datalight Inc.

1.3 Disclaimer

DIGITAL-LOGIC AG makes no representations or warranties with respect to the contents of this manual and specifically disclaims any implied warranty of merchantability or fitness for any particular purpose. DIGITAL-LOGIC AG shall under no circumstances be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage. DIGITAL-LOGIC AG reserves the right to revise this publication from time to time without obligation to notify any person of such revisions

1.4 Who should use this product

- Electronic engineers with know-how in PC-technology.
- Without electronic know-how we expect you to have questions. This manual assumes, that you have a general knowledge of PC-electronics.
- Because of the complexity and the variability of PC-technology, we can't give any warranty that the product will work in any particular situation or combination.
- Pay attention to the electrostatic discharges. Use a CMOS protected workplace.
- Power supply OFF when you are working on the board or connecting any cables or devices.

This is a high technology product.
You need know-how in electronics and PC-technology to install the system !

1.5 Recycling Information

Hardware:

- Print: epoxy with glass fiber
wires are of tin-plated copper

- Components: ceramics and alloys of gold, silver
check your local electronic recycling

1.6 SMART Support Request Form (SMART-SRF)

1. Send this SRF with your problem description to:

DIGITAL-LOGIC AG
smartModule DesignIn Center
Nordstr. 11/F
CH-4542 Luterbach (SWITZERLAND)
Fax: ++41 32 681 58 01
E-Mail: support@digitallogic.com
Internet www.digitallogic.com

Support request form (fill in and send via fax to DIGITAL-LOGIC AG support center):

SRF No:	**S118_____**		**Date:**	
Customer Name:			Customer company:	
Customer Tel.No.:			Customer E-Mail:	
Customers Address:			Customers Country:	
SMART type:	SM586PC		processing date:	
Request type:	Support Report:		Operating System:	
	DesignIn Aid:		OS Version:	V___.____
	BIOS Adaption:		BIOS Version:	V___.____
	Manual Correction:			
	others:			

Problem description:
Solution / Answer (will be filled in by DIGITAL-LOGIC AG SMART DesignIn center):

Support date:			Support statistics:	
Support sign:			Comment:	
Support cost:	yes no		Offered costs for serving design support:	CHF/USD/DEM:
DesignIn No.:			Effective time / costs:	

1.7 smart DesignIn Center (smart – DIC)

DIGITAL-LOGIC AG offers a DesignIn support from a specialized engineering group in the SMART DesignIn Center (SMART – DIC). To initialize a DesignIn Support, please fill in the SMART-SRF form. The DesignIn Support can be offered in each phase of a DesignIn procedure. Only the ordered support value will be charged. The charge fees are as follow:

Design Phase	No.	Support type	Fee	Charged
Evaluation	01	Consultation	CHF 200.--	per hour
	02	Training	CHF 200.--	per hour
	03	Design of the customers specification	CHF 150.--	per hour
Schematics	10	Consultation	CHF 200.--	per hour
	11	Design of the schematics	CHF 150.--	per hour
	12	Review / Inspection of customers schematics	CHF 300.--	per sheet
	13	Development of circuits / schematics	CHF 200.--	per hour
Layout	20	Consultation	CHF 200.--	per hour
	21	Design of the layout	CHF 150.--	per hour
	22	Review / Inspection of customers layout	CHF 300.--	per sheet
	23	Development of circuits / layout	CHF 200.--	per hour
BIOS	30	Consultation	CHF 200.--	per hour
	31	Modification / Test of the BIOS sourcecode	CHF 1500.--	per day
	32	Review / Inspection of customers software	CHF 300.--	per hour
	33	Development of software	CHF 200.--	per hour
Prototype	40	Consultation	CHF 200.--	per hour
	41	Test of customers system	CHF 1200.--	per day
	42	Review / Inspection of customers system	CHF 300.--	per hour
	43	Development of test entvironment	CHF 200.--	per hour

All costs are payable in advance.

1.8 Limited Warranty

DIGITAL-LOGIC AG warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

Before returning any product for repair, customers are required to contact the company.

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Neither, if the user has not enough knowledge of these technologies or has not consulted the product manual or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

Except, as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

1.9 Sample Design Schematics

DIGITAL-LOGIC AG offers all schematics as a design guide only. DIGITAL-LOGIC AG assumes no responsibility for final system design. It is also assumed, that the designer has the reference manual of the PENTIUM chip, the programmers reference from the PENTIUM chip. DIGITAL-LOGIC AG assumes, that the designer of a smartModule-586PC design, has the knowledge of designing ISA based PC architecture.

2 OVERVIEW

2.1 Features

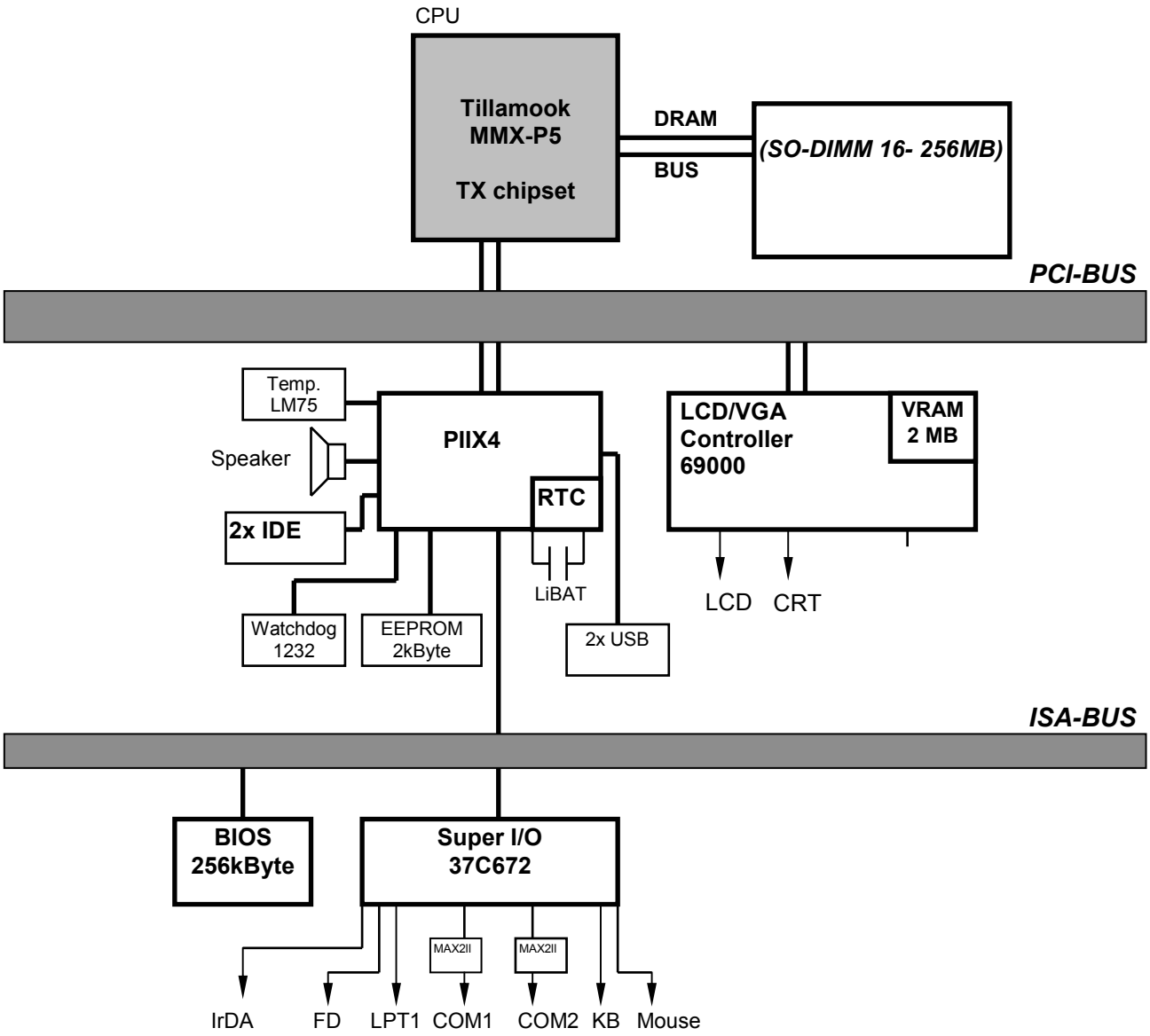
The smartModule-586PC is a miniaturized PC system on chip unit incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

- Powerful X86
- BIOS ROM (since V2.0 soldered)
- SODIMM socket for 16 - 128MB
- Timers
- DMA
- Real-time clock
- 2k EEPROM
- LPT1
- COM1, COM2
- Speaker interface
- AT-keyboard interface
- PS/2 mouse interface
- Floppydisk interface
- 2x ATA-IDE harddisk interface
- VGA/LCD video controller
- Embedded smartBUS480
- 3.3V power supply (switched mode)

2.2 Unique Features

- EEPROM for setup and configuration
- UL approved parts
-

2.3 SM586PC block diagram



2.4 Specifications

CPU:	
CPU:	MachZF 586 133MHz
Mode:	Real / Protected
Compatibility:	8086 – 80386
1. Level Cache:	16 & 16kByte write-back
Word Size:	64 Bits
Physical Addressing:	32 lines
Virtual Addressing:	64 Mbytes
Clock Rates:	133 MHz selectable
Math. Coprocessor:	
	Available on the CPU -
Power Management:	
available	Defined by the PHOENIX BIOS
DMA:	
8237A comp.	2 channels 8 Bits
Interrupts:	
8259 comp.	8 + 2 levels PC compatible
Timers:	
8254 comp.	3 programmable counter/timers
Memory:	
DRAM	SODIMM 144pin holder (16 – 128Mbyte), external expandable
Video:	
Controller:	69000 PCI-BUS CRT: 2Mbyte LCD: up to 1024 x 768 x 256 colors Panel: TFT 24Bit, STN, EL Plasma
Mass Storage:	
FD:	Floppy disk interface, for max. 2 floppy
HD:	2x IDE interface, AT - Type, for max. 4 harddisks

Standard AT Interfaces:

Serial:

Device Name	FIFO	Std.-IRQs	Addr.	Signals:	Remarks
COM1	yes	IRQ4	3F8		
COM2	yes	IRQ3	2F8		

(Baudrates: 50 – 115 KBaud programmable)

Parallel:	LPT1 printer interface, Modes: SPP (output) , EPP (bidir.)
Keyboard:	AT- or PS/2-keyboard
Mouse:	PS/2
Speaker:	0.1 W output drive
RTC:	Integrated into the PIIX4 with CMOS-RAM 256byte
Backup current:	<5 µA at 3V
Battery:	Not assembled

Supervisory:

Watchdog:	LTC1232 with power-fail detection, strobe time max. 1 sec.

BUS:

ISA:	IEEE-996 standard bus
Clock:	8 MHz
PC/104plus	IEEE-996 standard bus, buffered
Clock:	10 MHz defined by the PIIX4
USB	Defined by the PIIX4
DRAM	Defined by the PIIX4

Power Supply:

Working:	5 Volts ± 5%, 3.3V onboard switch mode regulator
Power Rise Time:	> 100µs (0V --> 4,75V)

Physical Characteristics:

Dimensions:	Length:	85 mm +/- 0.1mm
	Depth:	66 mm +/- 0.1mm
	Height:	16 mm +/- 0.2mm (with 5mm bus connectors)

Weight:	90 gr / 9 ounces
PCB Thickness:	1.6 mm / 0.0625 inches nominal
PCB Layer:	Multilayer

Operating Environment:

Relative Humidity:	5 - 90% non condensing	
Vibration:	5 to 2000 Hz	
Shock:	10 G	
Temperature:	Operating:	Standard version 166MHz: -25°C to +70**###**C (with a 266MHz only 60°C, or 70°C if clk reduced!) Extended version: -40°C to +85°C T.B.A
	Storage:	-55°C to +85 **###**C

EMI / EMC (IEC1131-2 refer MIL 461/462):	
ESD Electro Static Discharge:	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 metallic protection needed separate Ground Layer included 15 kV single peak
REF Radiated Electromagnetic Field:	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. not tested
EFT Electric Fast Transient (Burst):	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 ohms, Ts=5ns Grade 2: 1KV Supply, 500 I/O, 5Khz
SIR Surge Immunity Requirements:	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2 kV, 6 pulse/minute I/O: 500 V, 2 pulse/minute FD, CRT: none
High-frequency radiation:	EN55022

Any information is subject to change without notice.

2.5 Ordering Codes

SM586PC-133	smartModule586PC, 133MHz, 0MB
SMxxPC-DK-32	smartModulexxPC Development-Kit with 32Mbyte DRAM

2.6 BIOS History

Version:	Date:	Status:	Modifications:

2.7 This product is "YEAR 2000 CAPABLE"

This DIGITAL-LOGIC product is "YEAR 2000 CAPABLE". This means, that upon installation, it accurately stores, displays, processes, provides and/or receives date data from, into, and between 1999 and 2000, and the 20. and 21. centuries, including leap year calculations, provided that all other technology used in combination with said product properly exchanges date data with it. DIGITAL-LOGIC makes no representation about individual components within the product should be used independently from the product as a whole. You should understand that DIGITAL-LOGIC's statement that an DIGITAL-LOGIC product is "YEAR 2000 CAPABLE" means only that DIGITAL-LOGIC has verified that the product as a whole meets this definition when tested as a stand-alone product in a test lab, but does not mean that DIGITAL-LOGIC has verified that the product is "YEAR 2000 CAPABLE" as used in your particular situation or configuration. DIGITAL-LOGIC makes no representation about individual components, including software, within the product should they be used independently from the product as a whole.

DIGITAL-LOGIC customers use DIGITAL-LOGIC products in countless different configurations and in conjunction with many other components any systems, and DIGITAL-LOGIC has no way to test whether all those configurations and systems will properly handle the transition to the year 2000. DIGITAL-LOGIC encourages its customers and others to test whether their own computer systems and products will properly handle the transition to the year 2000.

The only proper method of accessing the date in systems is indirectly from the Real-Time-Clock via the BIOS. The BIOS in DIGITAL-LOGIC computerboards contains a century checking and maintenance feature the checks the laest two significant digits of the year stored in the RTC during each BIOS request (INT 1A) to read the date and, if less than '80' (i.e. 1980 is the first year supported by the PC), updates the century byte to '20'. This feature enables operating systems and applications using BIOS date/time services to reliably manipulate the year as a four-digit value.

2.8 Related Application Notes

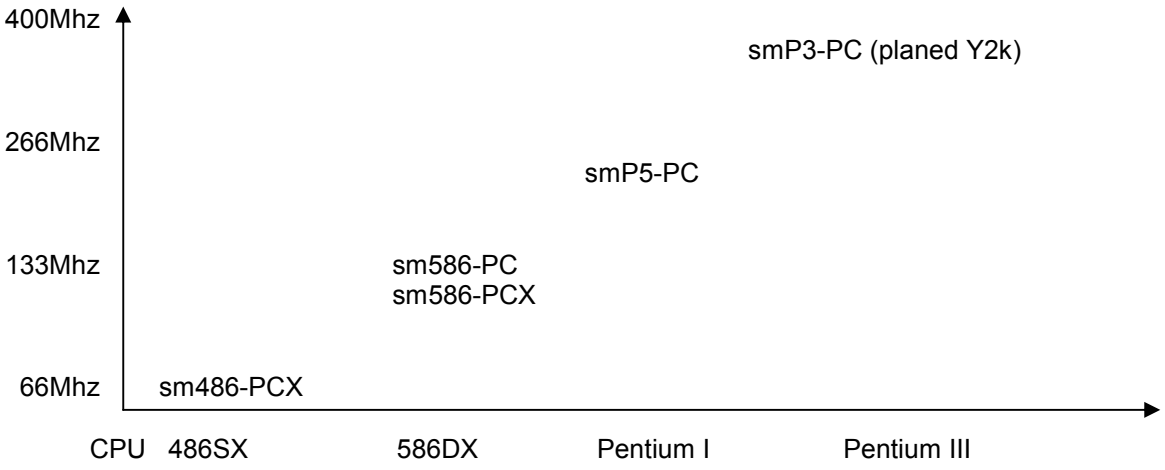
#	Description

➔ *Application Notes re availble at http://www.digitallogic.com ->support, or on any Application CD from DIGITAL-LOGIC.*

2.9 The smart480 bus , the future upgrade path

DIGITAL-LOGIC produces different smartmodules using the smart480 bus. Since each module has some unique features, the integrator must use this signals carefully, if he likes to upgrade lateron with another module with a higher performance.

The following performance will be available:



CPU	486SX (ELAN400)	586DX	Pentium I	Pentium III
CPU-Clock	**33-99Mhz**	**133Mhz**	**166-266Mhz**	**400-500Mhz**
Power consumption	**3 - 4 Watts**	**3 – 5 Watts**	**5 – 7 Watts**	**7 – 9 Watts**
Standard functions				
DRAM Expansion	32Bit	32Bit	64Bit	64Bit
Keyboard & Mouse	yes	yes	yes	yes
COM1	yes	yes	yes	yes
COM2	yes	yes	yes	yes
Floppydisk	yes	yes	yes	yes
LPT1	yes	yes	yes	yes
Prim-IDE	yes	yes	yes	yes
Sec-IDE	no	yes	yes	yes
ISA-Bus	yes	yes	yes	yes
CRT-VGA Signals	yes	yes	yes	yes
LCD 24Bit	yes	yes	yes	yes
Unique functions:				
PCCard	yes	no	no	no
LAN	yes	no	no	no
PCI-Bus	no	yes	yes	yes
Keymatrix	yes	no	no	no
1/4VGA LCD	yes	no	no	no
36Bit LCD Extension	no	yes	yes	yes
USB Interface	no	no	yes	yes
COM3	yes	no	no	no
ZV-Port	no	no	no	no

2.10 The smartModule586PC thermoanalysis

DIGITAL-LOGIC provides a set of thermal images, made after 60min operating in a typical applications.

Without cooler:

3 PC FUNCTIONAL DESCRIPTION

3.1 Interrupt Controllers

An 8259A compatible interrupt controller, within the TX chipset, provides seven prioritized interrupt levels. Of these, several are normally associated with the board's onboard device interfaces and controllers, and several are available on the AT expansion bus.

Interrupt:	Sources:	onboard used:
IRQ0	ROM-BIOS clock tick function, from timer 0	yes
IRQ1	Keyboard controller output buffer full	yes
IRQ2	Used for cascade 2. 8259	yes
IRQ3	COM2 serial port	yes
IRQ4	COM1 serial port	yes
IRQ5	LPT2 parallel printer (if present)	no *
IRQ6	Floppy controller	yes
IRQ7	LPT1 parallel printer	yes
IRQ8	Battery backed clock	yes
IRQ9	Free for user	no *
IRQ10	Free for user	no *
IRQ11	Free for user	no *
IRQ12	PS/2 mouse	yes
IRQ13	Math. coprocessor	yes
IRQ14	Harddisk IDE / SCSI	yes
IRQ15	Free for user	no *

- * It may depends on the LAN configuration

3.2 Timers and Counters

3.2.1 Programmable Timers

An 8253 compatible timer/counter device is also included in the board's ASIC device. This device is utilized in precisely the same manner as in a standard AT implementation. Each channel of the 8253 is driven by a 1.190 MHz clock, derived from a 14.318 MHz oscillator, which can be internally divided in order to provide a variety of frequencies.

Timer 2 can also be used as a general purpose timer if the speaker function is not required.

Timer Assignment

Timer	Function
0	ROM-BIOS clock tick (18.2 Hz)
1	DRAM refresh request timing (15 µs)
2	Speaker tone generation time base

3.2.2 Battery backed clock (RTC)

An AT compatible date/time clock is located within the chipset. The device also contains a CMOS static RAM, compatible with that in standard ATs. System configuration data is normally stored in the clock chip's CMOS RAM in a manner consistent with the convention used in other AT compatible computers.

Connect an external Lithium battery of 3V to the RTC pin.

The battery-backed clock can be set by using the DIGITAL-LOGIC AG SETUP at boot-time.

Addresses:	70h	=	Index register
	71h	=	Data transfer register
RTC-Address MAP:	00 - 0F		Real time clock
	10 - 3F		BIOS setup (Standard)
	40 - 7F		Extended BIOS

With an external Lithium 3V- battery, the board is able to work over 10 years without replacing. The chip set consumes the following currents:

Typical battery current at 25°C : <5 µA

3.2.3 Watchdog

3.3 BIOS

3.3.1 ROM-BIOS

An EPROM with 8 Bit wide data access normally contains the board's AT compatible ROM-BIOS. The BIOS takes a 29C020 EPROM (or equivalent) device. The board's wait-state control logic automatically inserts four memory wait states in all CPU accesses to this (socket). The ROM-BIOS occupies the memory area from C0000H through FFFFFh; however, the board's ASIC logic reserves the entire area from C0000h through FFFFFh for onboard devices, so that this area is already usable for ROM-DOS and BIOS expansion modules.
Consult the appropriate address map for the MICROSPACE SM586PC ROM-BIOS.

3.3.1.1 Standard BIOS ROM

DEVICE:	29C020 PLCC32	
MAP:	E0000 - FFFFFh	BIOS from PHOENIX, 256kB onboard soldered
	C0000 - CBFFFh	VGA BIOS from Chips & Technology 32kB or 44kB
	CC000 - CFFFFh	reserved

3.3.2 EEPROM Memory for Setup

The EEPROM is used for setup and configuration data, stored as an alternative to the CMOS-RTC. Optionally, the EEPROM setup driver may update the CMOS RTC, if the battery is running down and the checksum error would appear and stop the system. The capacity of the EEPROM is 2 kByte.

Organisation of the 2048Byte EEPROMs:

Address MAP:	Function:
0000h	**CMOS-Setup valid (01=valid)**
0001h	**Keymatrix-Setup valid (01=valid)**
0003h	**Flag for DLAG-Message (FF=no message)**
0010h-007Fh	**Copy of CMOS-Setup data**
0080h-00FFh	**reserved for AUX-CMOS-Setup**
0100h-010Fh	**Serial-Number**
0110h-0113h	Production date (year/day/month)
0114h-0117h	1. Service date (year/day/month)
0118h-011Bh	2. Service date (year/day/month)
011Ch-011Fh	3. Service date (year/day/month)
0120h-0122h	Booterrors (Autoincremented if any booterror occurs)
0123h-0125h	Setup Entries (Autoincremented on every Setup entry)
0126h-0128h	Low Battery (Autoincremented everytime the battery is low, EEPROM -> CMOS)
0129h-012Bh	Startup (Autoincremented on every poweron start)
0130h	Number of 512k SRAM
0131h	Number of 512k Flash
0132h/0133h	BIOS Version (V1.4 => [0132h]:= 4, [0133h]:=1)
0134h/0135h	BOARD Version (V1.5 => [0124h]:=5, [0125h]:=1)
0136h	BOARD TYPE (‘M’=PC/104, ‘E’=Euro, ‘W’=MSWS, ‘S’=Slot, ‘C’=Custom)
0137h	CPU TYPE (01h=ELAN300/310, 02h=ELAN400, 03h=486SLC, 04h=486DX, 05h=P5).
0200h-03FFh	**Keymatrix-Setup data**
0200h-027Fh	Keymatrix Table
0400h-07FFh	**Free for Customer’s use**

3.3.3 BIOS CMOS Setup

If wrong setups are memorized in the CMOS-RAM, the default values will be loaded after resetting the RTC/CMOS-RAM with the CMOS-RESET jumper. If the battery is down, it is always possible to start the system with the default values from the BIOS.

WARNING:

On the next setup pages (switch with TAB) the values for special parameters are modifiable. Normally the parameters are set correctly by DIGITAL-LOGIC AG. Be very careful in modifying any parameter since the system could crash. Some parameters are dependent on the CPU type. The cache parameter is always available, for example. So, if you select too few wait states, the system will not start until you reset the CMOS-RAM using the RAM-Reset jumper, but the default values are reloaded. If you are not familiar with these parameters, do not change anything!

3.3.4 CMOS Setup Harddisk List

Use type 48 and type 49 for user defined harddisk entries. Enter the sectors, cylinders and the number of heads. Select AUTODETECT in order to autoidentify the harddisk parameters.

3.4 CMOS RAM Map

Systems based on the industry-standard specification include a battery backed Real Time Clock chip. This clock contains at least 64 bytes of non-volatile RAM. The system BIOS uses this area to store information including system configuration and initialization parameters, system diagnostics, and the time and date. This information remains intact even when the system is powered down.

The BIOS supports 128 bytes of CMOS RAM. This information is accessible through I/O ports 70h and 71h. CMOS RAM can be divided into several segments:

- Locations 00h - 0Fh contain real time clock (RTC) and status information
- Locations 10h - 2Fh contain system configuration data
- Locations 30h - 3Fh contain System BIOS-specific configuration data as well as chipset-specific information
- Locations 40h - 7Fh contain chipset-specific information as well as power management configuration parameters

The following table provides a summary of how these areas may be further divided.

Beginning	Ending	Checksum	Description
00h	0Fh	No	RTC and Checksum
10h	2Dh	Yes	System Configuration
2Eh	2Fh	No	Checksum Value of 10h - 2Dh
30h	33h	No	Standard CMOS
34h	3Fh	No	Standard CMOS - SystemSoft Reserved
40h	5Bh	Yes	Extended CMOS - Chipset Specific
5Ch	5Dh	No	Checksum Value of 40h - 5Bh
5Eh	6Eh	No	Extended CMOS - Chipset Specific
6Fh	7Dh	Yes	Extended CMOS - Power Management
7Eh	7Fh	No	Checksum Value of 6Fh - 7Dh

Location	Description
00h	Time of day (seconds) specified in BCD
01h	Alarm (seconds) specified in BCD
02h	Time of Day (minutes) specified in BCD
03h	Alarm (minutes) specified in BCD
04h	Time of Day (hours) specified in BCD
05h	Alarm (hours) specified in BCD
06h	Day of week specified in BCD
07h	Day of month specified in BCD
08h	Month specified in BCD
09h	Year specified in BCD
0Ah	Status Register A Bit 7 = Update in progress Bits 6-4 = Time based frequency divider Bits 3-0 = Rate selection bits that define the periodic interrupt rate and output frequency.
0Bh	Status Register B Bit 7 = Run/Halt 0 Run 1 Halt Bit 6 = Periodic Timer 0 Disable 1 Enable Bit 5 = Alarm Interrupt 0 Disable 1 Enable Bit 4 = Update Ended Interrupt 0 Disable 1 Enable Bit 3 = Square Wave Interrupt 0 Disable 1 Enable Bit 2 = Calendar Format 0 BCD 1 Binary Bit 1 = Time Format 0 12-Hour 1 24-Hour Bit 0 = Daylight Savings Time 0 Disable 1 Enable
0Ch	Status Register C Bit 7 = Interrupt Flag Bit 6 = Periodic Interrupt Flag Bit 5 = Alarm Interrupt Flag Bit 4 = Update Interrupt Flag Bits 3-0 = Reserved
0Dh	Status Register D Bit 7 = Real Time Clock 0 Lost Power 1 Power

Continued...

CMOS Map Continued...

Location	Description
0Eh	CMOS Location for Bad CMOS and Checksum Flags bit 7 = Flag for CMOS Lost Power 0 = Power OK 1 = Lost Power bit 6 = Flag for CMOS checksum bad 0 = Checksum is valid 1 = Checksum is bad
0Fh	Shutdown Code
10h	Diskette Drives bits 7-4 = Diskette Drive A 0000 = Not installed 0001 = Drive A = 360 K 0010 = Drive A = 1.2 MB 0011 = Drive A = 720 K 0100 = Drive A = 1.44 MB 0101 = Drive A = 2.88 MB bits 3-0 = Diskette Drive B 0000 = Not installed 0001 = Drive B = 360 K 0010 = Drive B = 1.2 MB 0011 = Drive B = 720 K 0100 = Drive B = 1.44 MB 0101 = Drive B = 2.88 MB
11h	Reserved
12h	Fixed (Hard) Drives bits 7-4 = Hard Drive 0, AT Type 0000 = Not installed 0001-1110 Types 1 - 14 1111 = Extended drive types 16-44. See location 19h. bits 3-0 = Hard Drive 1, AT Type 0000 = Not installed 0001-1110 Types 1 - 14 1111 = Extended drive types 16-44. See location 2Ah. See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
13h	Reserved

Continued...

CMOS Map Continued...

Location	Description
14h	Equipment bits 7-6 = Number of Diskette Drives 00 = One diskette drive 01 = Two diskette drives 10, 11 = Reserved bits 5-4 = Primary Display Type 00 = Adapter with option ROM 01 = CGA in 40 column mode 10 = CGA in 80 column mode 11 = Monochrome bits 3-2 = Reserved bit 1 = Math Coprocessor Presence 0 = Not installed 1 = Installed bit 0 = Bootable Diskette Drive 0 = Not installed 1 = Installed
15h	Base Memory Size (in KB) - Low Byte
16h	Base Memory Size (in KB) - High Byte
17h	Extended Memory Size in (KB) - Low Byte
18h	Extended Memory Size (in KB) - High Byte
19h	Extended Drive Type - Hard Drive 0 See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
1Ah	Extended Drive Type - Hard Drive 1 See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
1Bh	Custom and Fixed (Hard) Drive Flags bits 7-6 = Reserved bit 5 = Internal Floppy Diskette Controller 0 = Disabled 1 = Enabled bit 4 = Internal IDE Controller 0 = Disabled 1 = Enabled bit 3 = Hard Drive 0 Custom Flag 0 = Disable 1 = Enabled bit 2 = Hard Drive 0 IDE Flag 0 = Disable 1 = Enabled bit 1 = Hard Drive 1 Custom Flag 0 = Disable 1 = Enabled bit 0 = Hard Drive 1 IDE Flag 0 = Disable 1 = Enabled

Continued...

CMOS Map Continued...

Location	Description
1Ch	Reserved
1Dh	EMS Memory Size Low Byte
1Eh	EMS Memory Size High Byte
1Fh - 24h	Custom Drive Table 0 These 6 bytes (48 bits) contain the following data: Cylinders Landing Zone 10 bits Write Precomp 10 bits Heads Sectors/Track 8 bits
1Fh	Byte 0 bits 7-0 = Lower 8 Bits of Cylinders
20h	Byte 1 bits 7-2 = Lower 6 Bits of Landing Zone bits 1-0 = Upper 2 Bits of Cylinders
21h	Byte 2 bits 7-4 = Lower 4 Bits of Write Precompensation bits 3-0 = Upper 4 Bits of Landing Zone
22h	Byte 3 bits 7-6 = Reserved bits 5-0 = Upper 6 Bits of Write Precompensation
23h	Byte 4 bits 7-0 = Number of Heads
24h	Byte 5 bits 7-0 = Sectors Per Track
25h - 2Ah	Custom Drive Table 1 These 6 bytes (48 bits) contain the following data: Cylinders Landing Zone 10 bits Write Precomp 10 bits Heads Sectors/Track 8 bits
25h	Byte 0 bits 7-0 = Lower 8 Bits of Cylinders
26h	Byte 1 bits 7-2 = Lower 6 Bits of Landing Zone bits 1-0 = Upper 2 Bits of Cylinders
27h	Byte 2 bits 7-4 = Lower 4 Bits of Write Precompensation bits 3-0 = Upper 4 Bits of Landing Zone

Continued...

CMOS Map Continued...

Location	Description
28h	Byte 3 bits 7-6 = Reserved bits 5-0 = Upper 6 Bits of Write Precompensation
29h	Byte 4 bits 7-0 = Number of Heads
2Ah	Byte 5 bits 7-0 = Sectors Per Track
2Bh	Boot Password bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password bits 6-0 = Calculated Password
2Ch	SCU Password bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password bits 6-0 = Calculated Password
2Dh	Reserved
2Eh	High Byte of Checksum - Locations 10h to 2Dh
2Fh	Low Byte of Checksum - Locations 10h to 2Dh
30h	Extended RAM (KB) detected by POST - Low Byte
31h	Extended RAM (KB) detected by POST - High Byte
32h	BCD Value for Century
33h	Base Memory Installed bit 7 = Flag for Memory Size 0 = 640KB 1 = 512KB bits 6-0 = Reserved
34h	Minor CPU Revision Differentiates CPUs within a CPU type (i.e., 486SX vs 486 DX, vs 486 DX/2). This is crucial for correctly determining CPU input clock frequency. During a power on reset, Reg DL holds minor CPU revision.
35h	Major CPU Revision Differentiates between different CPUs (i.e., 386, 486, Pentium). This is crucial for correctly determining CPU input clock frequency. During a power on reset, Reg DH holds major CPU revision.
36h	Hotkey Usage bits 7-6 = Reserved bit 5 = Semaphore for Completed POST bit 4 = Semaphore for 0 Volt POST (not currently used) bit 3 = Semaphore for already in SCU menu bit 2 = Semaphore for already in PM menu bit 1 = Semaphore for SCU menu call pending bit 0 = Semaphore for PM menu call pending
40h-7Fh	Definitions for these locations vary depending on the chipset.

3.4.1 Harddisk PIO Modes

Block Mode Transfer: (Multi-Sector)

Block mode boots IDE drive performance by increasing the amount of data transferred.

No Block Mode: 512 Byte per interrupt
Block Mode: up to 64 kByte per interrupt

LBA Mode:

LBA (logical block addressing) is a new method of addressing data on a disk drive. In the standard ST506 (MFM) ISA hard disk, data is accessed via a cylinder - head - sector format.

LBA Mode disabled: max. 528 MByte per Disk

LBA Mode enabled: max. 8 Gbyte per Disk

Attention:
The BIOS enables the LBA Mode only, if the harddisk was formatted on a system with enabled LBA. If the drive (capacity > 528MB) is formatted on a system with disabled LBA, the PHOENIX BIOS will never enable the LBA mode !

The maximum parameters are:
1024 Cyl., 16 heads, 63 Sec/Track

32Bit Transfer:

Some operating system can handle two 16Bit word as one 32Bit access. This accelerates the IDE transfer.

Advanced PIO Modes:

	PIO-Mode:	Timing:	Transferspeed:	Remarks:
IDE	0	600ns	2 MByte/sec	Slowest I/O
IDE	1	383ns	5.5MByte/sec	Standard I/O
EIDE	2	240ns	8.3MByte/sec	Fast I/O, Mem.
EIDE	3	180ns	11,3MByte/sec	IORDY Protocol
EIDE	4	120ns	16,6MByte/sec	IORDY Protocol
EIDE	DMA 1	160ns	13,3MByte/sec	DRQ, ATA-2

Warning: **Always begin with the PIO-Mode 0 in the manual mode (not autodetect) to test a new drive or if you have troubles in the automatic mode. The autodetect mode of some drives select wrong PIO modes.**

3.5 EEPROM saved CMOS Setup

The EEPROM has different functions, as listed below:

- Backup of the CMOS-Setup values.
- Storing system informations like: version, production date, customisation of the board, CPU type.
- Storing user/application values.

The EEPROM will be updated automatically after exiting the BIOS setup menu. The system will operate also without any CMOS battery. While booting up, the CMOS is automatically updated with the EEPROM values.

If the system hangs or a problem appears, the following steps must be performed:

1. Reset the CMOS-Setup (use the jumper to reset or disconnect the battery for at least 10 minutes).
2. Press Esc until the system starts up.
3. Enter the BIOS Setup:
   a) load DEFAULT values
   b) enter the settings for the environment
   c) exit the setup
4. Restart the system.

- The user may access the EEPROM through the INT15 special functions. Refer to the chapter SFI functions 3.10.1.
- The system information are read only information. To read, use the SFI functions.

3.6 Download the VGA-BIOS and the CORE-BIOS

Before downloading a BIOS, please check as follows:

- Select the SHADOW option in the BIOS, for a BIOS and VGA (if this option is available).
- Disable the EMM386 or other memory managers in the CONFIG.SYS of your bootdisk.
- Make sure, that the DOWN_xxx.EXE programm and the BIOS to download are on the same path and directory!
- Boot the DOS without config.sys & autoexec.bat -> press “F5” while starting DOS boot.
- Is the empty diskspace, where the down.exe is located, larger than 64kB (for safe storage)
- Is the floppydisk not write-protected

Start the DOWNLOADING Tool with:

- Start the corresponding download tool. Refer to the table to see which tool fits in, each productgroup has its own download tool. Do never use the wrong one!

Product:	BIOS-Core download	VGA-BIOS download	BIOS-Ext. download
File-Extension:	*.COR	*.V40 , *.V45 *.V48 depending on the product	*.BIN
BIOS Size:	128k	32k	32k
Addressrange:	E0000 - FFFFFh	C0000 – C7FFFh	C8000 - CFFFFh
MSM386SN	DOWN_3SN.EXE	-	-
MSM386SV	DOWN_3SV.EXE	DOWN_3SV.EXE	DOWN_3SV.EXE
MSM486SL	DOWN_4SN.EXE	-	-
MSM486SN	DOWN_4SN.EXE	-	-
MSM486SV	DOWN_4SV.EXE	DOWN_4SV.EXE	DOWN_4SV.EXE
MSM486SE / SEV	DOWN_4SE.EXE	DOWN_4SE.EXE	-
MSM486DN	DOWN_4DX.EXE	-	-
MSM486DX	DOWN_4DX.EXE	DOWN_4DX.EXE	DOWN_4DX.EXE
SM-486PC / EK	DOWN_SM4.EXE	On the –EK : DOWN_SM4.EXE	-
SM-486PCX / EK	DOWN_S4X.EXE	DOWN_S4X.EXE	DOWN_S4X.EXE
MSM5x86DX	DOWN_4DX.EXE	DOWN_4DX.EXE	DOWN_4DX.EXE
MSM-P5	- AMI82602.EXE or - FLASHAMI.COM (AMIBOOT.ROM)**	DOWN_000.EXE	-
PCC-P5L PCC-PII AMI- BIOS	AMI82602.EXE	DOWN_000.EXE	-
PCC-P5L PCC-PII PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	-
MSM-P5S	AMI82602.EXE	DOWN_000.EXE	-
MSM-P5SV / SEV AMI- BIOS	AMI82602.EXE	DOWN_000.EXE	-
MSM-P5SN / SEN AMI- BIOS	AMI82602.EXE	-	-
MSM-P5SV / SEV PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	-
MSM-P5SN / SEN PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	-	-
SMP5PC / DK	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	
MAS-P5	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	

Remarks:
** Core- file has to be renamed as written in brackets

3.6.1 VGA BIOS Download Function

The BIOS for the VGA must be downloaded, before a LCD is connected. This could be also a new LCD- display, which needs a corresponding VGA- BIOS.

See als chapter **Application to use the downloadtool for the external VGA BIOS**
in our INTEGRATION MANUAL

How to download a VGA- BIOS:

1. Restart the system with the SHADOW enabled (if available) and no EMM386 loaded.
2. Check, if you find the DOWN_xxx.EXE and the *.V40 / *.000 files on your disk, to get downloaded.
3. Refer to the VGABIOS.DOC for more information about the VGABIOS files.
4. Insert the floppydisk with the program DOWN_xxx.EXE and all VGA-Drivers.
5. Start DOWN_xxx.EXE.
6. Check, if the DOWN program has identified the product and the shadow correctly.
7. Select the function PROGRAMM VGA- BIOS.
8. Select the VGA- BIOS out of the proposed file list (UP/DOWN arrows) and press ENTER.
9. Check, if the new VGA- header is displayed on the VGA- INFO- screen.
10. After proceeding, switch off the power and restart the board (cold start).

If the download does not work:

- Check, if no EMM386 is loaded.
- Check, if no peripheral card is in the system, which occupies the same memory range. Disconnect this card.
- If the download is stopped or not completed, make only a warm boot and repeat the steps or download another file. As the video is may shadowed, everything is visible and a cold boot would clear the screen and nothing would be visible afterwards.

If the screen flickers or is misaligned after reboot:

- The previously loaded VGA- BIOS is not corresponding 100% or works only on the LCD properly.

If the screen is dark after the reboot of the system:

- A new system BIOS must be programmed. Ask DIGITAL-LOGIC AG for the binary file.

If the previous version is still programmed:

- Switch off the board and do not make a warm boot due to the fact that the data may are still in the shadow stored.

3.7 Memory

3.7.1 System Memory Map

The PENTIUM™ CPU used as central processing unit on the MICROSPACE has a memory address space which is defined by 32 address bits. Therefore, it can address 1 GByte of memory. The memory address MAP is as follows:

CPU Pentium

Address:	Size:	Function / Comments:
000000 - 09FFFFh	640 KBytes	Onboard DRAM for DOS applications
0A0000 - 0BFFFFh	128 KBytes	CGA, EGA, LCD Video RAM 128kB
0C0000 - 0CBFFFh	48 KBytes	VGA BIOS selected by the hardware
0CC000 - 0CFFFFh	16 KBytes	BIOS extensions selected by the hardware
0D0000 - 0D4000h	16 KBytes	free for user
0D4000 - 0D8000h	16 KBytes	free for user
0D8000 - 0DFFFFh	32 KBytes	free for user
0E0000 - 0EFFFFh	64 KBytes	PHOENIX BIOS selected by the PIIX4 chipset
0F0000 - 0FFFFFh	64 KBytes	PHOENIX BIOS selected by the PIIX4 chipset
100000 - 1FFFFFh	1 MByte	DRAM for extended onboard memory
200000 - FFFFFFh	14 MBytes	DRAM for extended onboard memory

3.7.2 System I/O map

The following table shows the detailed listing of the I/O port assignments used in the MICROSPACE board:

I/O Address	Read/Write Status	Description
0000h	R / W	DMA channel 0 address byte 0 (low), then byte 1
0001h	R / W	DMA channel 0 word count byte 0 (low), then byte 1
0002h	R / W	DMA channel 1 address byte 0 (low), then byte 1
0003h	R / W	DMA channel 1 word count byte 0 (low), then byte 1
0004h	R / W	DMA channel 2 address byte 0 (low), then byte 1
0005h	R / W	DMA channel 2 word count byte 0 (low), then byte 1
0006h	R / W	DMA channel 3 address byte 0 (low), then byte 1
0007h	R / W	DMA channel 3 word count byte 0 (low), then byte 1
0008h	R	DMA channel 0-3 status register bit 7 = 1 Channel 3 request bit 6 = 1 Channel 2 request bit 5 = 1 Channel 1 request bit 4 = 1 Channel 0 request bit 3 = 1 Terminal count on channel 3 bit 2 = 1 Terminal count on channel 2 bit 1 = 1 Terminal count on channel 1 bit 0 = 1 Terminal count on channel 0

Continued...

I/O Address	Read/Write Status	Description
0008h	W	DMA channel 0-3 command register bit 7 = DACK sense active high/low 0 low 1 high bit 6 = DREQ sense active high/low 0 low 1 high bit 5 = Write selection 0 Late write selection 1 Extended write selection bit 4 = Priority 0 Fixed 1 Rotating bit 3 = Timing 0 Normal 1 Rotating bit 2 = Controller enable/disable 0 Enable 1 Disable bit 1 = Memory-to-memory enable/disable 0 Disable 1 Enable bit 0 = Reserved
0009h	W	DMA write request register
000Ah	R / W	DMA channel 0-3 mask register bits 7-3 = Reserved bit 2 = 0 Clear bit 1 Set bit bits 1-0 = Channel Select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3
00Bh	W	DMA channel 0-3 mode register bits 7-6 = 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode bit 5 = 0 Address increment select 1 Address decrement select bit 4 = 0 Disable auto initialization 1 Enable auto initialization bits 3-2 = Operation type 00 Verify operation 01 Write to memory 10 Read from memory 11 Reserved bits 1-0 = Channel select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3

Continued...

I/O Address	Read/Write Status	Description
000Ch	W	DMA clear byte pointer flip/flop
000Dh	R	DMA read temporary register
000Dh	W	DMA master clear
000Eh	W	DMA clear mask register
000Fh	W	DMA write mask register
0020h	W	Programmable Interrupt Controller - Initialization Command Word 1 (ICW1) provided bit 4 = 1 bits 7-5 = 000 Used only in 8080 or 8085 mode bit 4 = 1 ICW1 is used bit 3 = 0 Edge triggered mode 1 Level triggered mode bit 2 = 0 Successive interrupt vectors separated by 8 bytes 1 Successive interrupt vectors separated by 4 bytes bit 1 = 0 Cascade mode 1 Single mode bit 0 = 0 ICW4 not needed 1 ICW4 needed
0021h	W	Used for ICW2, ICW3, or ICW4 in sequential order afterICW1 is written to port 0020h **ICW2** bits 7-3 = Address A0-A3 of base vector address for interrupt controller bits 2-0 = Reserved (should be 000) **ICW3** (for slave controller 00A1h) bits 7-3 = Reserved (should be 0000) bits 2-0 = 1 Slave ID **ICW4** bits 7-5 = Reserved (should be 000) bit 4 = 0 No special fully nested mode 1 Special fully nested mode bits 3-2 = Mode 00 Non buffered mode 01 Non buffered mode 10 Buffered mode/slave 11 Buffered mode/master bit 1 = 0 Normal EOI 1 Auto EOI bit 0 = 0 8085 mode 1 8080 / 8088 mode

Continued...

I/O Address	Read/Write Status	Description
0021h	R / W	PIC master interrupt mask register (OCW1) bit 7 = 0 Enable parallel printer interrupt bit 6 = 0 Enable diskette interrupt bit 5 = 0 Enable hard disk interrupt bit 4 = 0 Enable serial port 1 interrupt bit 3 = 0 Enable serial port 2 interrupt bit 2 = 0 Enable video interrupt bit 1 = 0 Enable kybd/pointing device/RTC interrupt bit 0 = 0 Enable interrupt timer
0021h	W	PIC OWC2 (if bits 4-3 = 0) bit 7 = Reserved bits 6-5 = 000 Rotate in automatic EOI mode (clear) 001 Nonspecific EOI 010 No operation 011 Specific EOI 100 Rotate in automatic EOI mode (set) 101 Rotate on nonspecific EOI command 110 Set priority command 111 Rotate on specific EOI command bits 4-3 = Reserved (should be 00) bits 2-0 = Interrupt request to which the command applies
0020h	R	PIC interrupt request and in-service registers programmed by OCW3 **Interrupt request register** bits 7-0 = 0 No active request for the corresponding interrupt line 1 Active request for the corresponding interrupt line **Interrupt in-service register** bits 7-0 = 0 Corresponding interrupt line not currently being serviced 1 Corresponding interrupt line is currently being serviced
0021h	W	PIC OCW3 (if bit 4 = 0, bit 3 = 1) bit 7 = Reserved (should 0) bits 6-5 = 00 No operation 01 No operation 10 Reset special mask 11 Set special mask bit 4 = Reserved (should be 0) bit = Reserved (should be 1) bit 2 = 0 No poll command 1 Poll command bits 1-0 = 00 No operation 01 Operation 10 Read interrupt request register on next read at port 0020 h 11 Read interrupt in-service register on next read at port 0020h

Continued...

I/O Address	Read/Write Status	Description
0022h	R / W	Chipsset Register Address
0023h	R / W	Chipsset Register Data
0040h	R / W	Programmable Interrupt Time read/write counter 0, keyboard controller channel 0
0041h	R / W	Programmer Interrupt Timer channel 1
0042h	R / W	Programmable Interrupt Timer miscellaneous register channel 2
0043h	W	Programmable Interrupt Timer mode port - control word register for counters 0 and 2 bits 7-0 = Counter select 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select bits 5-4 = 00 Counter latch command 01 R / W counter, bits 0-7 only 10 R / W counter, bits 8-15 only 11 R / W counter, bits 0-7 first, then bits 8-15 bits 3-1 = Select mode 000 Mode 0 001 Mode 1 programmable one shot x10 Mode 2 rate generator x11 Mode 3 square wave generator 100 Mode 4 software-triggered strobe 101 Mode 5 hardware-triggered strobe bit 0 = 0 Binary counter is 16 bits 1 Binary counter decimal (BCD) counter
0048h	R / W	Programmable interrupt timer
0060h	R	Keyboard controller data port or keyboard input buffer
0060h	W	Keyboard or keyboard controller data output buffer

Continued...

I/O Address	Read/Write Status	Description
0064h	R	Keyboard controller read status bit 7 = 0 No parity error 1 Parity error on keyboard transmission bit 6 = 0 No timeout 1 Received timeout bit 5 = 0 No timeout 1 Keyboard transmission timeout bit 4 = 0 Keyboard inhibited 1 Keyboard not inhibited bit 3 = 0 Data 1 Command bit 2 = System flag status bit 1 = 0 Input buffer empty 1 Input buffer full bit 0 = 0 Output buffer empty 1 Output buffer full
0064h	W	Keyboard controller input buffer
0070h	R	CMOS RAM index register port and NMI mask bit 7 = 1 NMI disabled bits 6-0 = 0 CMOS RAM index
0071h	R / W	CMOS RAM data register port
0080h	R / W	Temporary storage for additional page register
0080h	R	Manufacturing diagnostic port (this port can access POST checkpoints)
0081h	R / W	DMA channel 2 address byte 2
0082h	R / W	DMA channel 2 address byte 2
0083h	R / W	DMA channel 1 address byte 2
0084h	R / W	Extra DMA page register
0085h	R / W	Extra DMA page register
0086h	R / W	Extra DMA page register
0087h	R / W	DMA channel 0 address byte 2
0088h	R / W	Extra DMA page register
0089h	R / W	DMA channel 6 address byte 2
008Ah	R / W	DMA channel 7 address byte 2
008Bh	R / W	DMA channel 5 address byte 2
008Ch	R / W	Extra DMA page register
008Dh	R / W	Extra DMA page register
008Eh	R / W	Extra DMA page register
008Fh	R / W	DMA refresh page register

Continued...

I/O Address	Read/Write Status	Description
00A0h - 00A1h are reserved for the slave programmable interrupt controller. The bit definitions are identical to those of addresses 0020h - 0021h except where indicated.		
00A0h	R / W	Programmable interrupt controller 2
00A1h	R / W	Programmable interrupt controller 2 mask bit 7 = 0 Reserved bit 6 = 0 Enable hard disk interrupt bit 5 = 0 Enable coprocessor execution interrupt bit 4 = 0 Enable mouse interrupt bits 3-2 = 0 Reserved bit 1 = 0 Enable redirect cascade bit 0 = 0 Enable real time clock interrupt
00C0h	R / W	DMA channel 4 memory address bytes 1 and 0 (low)
00C2h	R / W	DMA channel 4 transfer count bytes 1 and 0 (low)
00C4h	R / W	DMA channel 5 memory address bytes 1 and 0 (low)
00C6h	R / W	DMA channel 5 transfer count bytes 1 and 0 (low)
00C8h	R / W	DMA channel 6 memory address bytes 1 and 0 (low)
00CAh	R / W	DMA channel 6 transfer count bytes 1 and 0 (low)
00CCh	R / W	DMA channel 7 memory address bytes 1 and 0 (low)
00CEh	R / W	DMA channel 7 transfer count bytes 1 and 0 (low)
00D0h	R	Status register for DMA channels 4-7 bit 7 = 1 Channel 7 request bit 6 = 1 Channel 6 request bit 5 = 1 Channel 5 request bit 4 = 1 Channel 4 request bit 3 = 1 Terminal count on channel 7 bit 2 = 1 Terminal count on channel 6 bit 1 = 1 Terminal count on channel 5 bit 0 = 1 Terminal count on channel 4
00D0h	W	Command register for DMA channels 4-7 bit 7 = 0 DACK sense active low 1 DACK sense active high bit 6 = 0 DREQ sense active low 1 DREQ sense active high bit 5 = 0 Late write selection 1 Extended write selection bit 4 = 0 Fixed Priority 1 Rotating Priority bit 3 = 0 Normal Timing 1 Rotating Timing bit 2 = 0 Enable controller 1 Disable controller bit 1 = 0 Disable memory-to-memory transfer 1 Enable memory-to-memory transfer bit 0 = Reserved

Continued...

I/O Address	Read/Write Status	Description
00D2h	W	Write request register for DMA channels 4-7
00D4h	W	Write single mask register bit for DMA channels 4-7 bits 7-3 = 0 Reserved bit 2 = 0 Clear mask bit, 1 Set mask bit bits 1-0 = Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D6h	W	Mode register for DMA channels 4-7 bits 7-6 = 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode bit 5 = 0 Address increment select 1 Address decrement select bit 4 = 0 Disable auto initialization 1 Enable auto initialization bits 3-2 = Operation type 00 Verify operation 01 Write to memory 10 Read from memory 11 Reserved bits 1-0 = Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D8h	W	Clear byte pointer flip/flop for DMA channels 4-7
00DAh	R	Read Temporary Register for DMA channels 4-7
00DAh	W	Master Clear for DMA channels 4-7
00DCh	W	Clear mask register for DMA channels 4-7
00DEh	W	Write mask register for DMA channels 4-7
00F0h	W	Math coprocessor clear busy latch
00F1h	W	Math coprocessor reset
00F2h - 00FFh	R / W	Math coprocessor
0140h – 014Fh	R / W	SCSI Controller if installed
I/O addresses 0170h - 0177h are reserved for use with a secondary hard drive. See addresses 01F0h - 01F7h for bit definitions.		
0170h	R / W	Data register for hard drive 1
0171h	R	Error register for hard drive 1
0171h	W	Precomposition register for hard drive 1
0172h	R / W	Sector count - hard drive 1

Continued...

I/O Address	Read/Write Status	Description
0173h	R / W	Sector number for hard disk 1
0174h	R / W	Number of cylinders (low byte) for hard drive 1
0175h	R / W	Number of cylinders (high byte) for hard drive 1
0716h	R / W	Drive/head register for hard drive 1
0177h	R	Status register for hard drive 1
0177h	W	Command register for hard drive 1
01F0h	R / W	Data register base port for hard drive 0
01F1h	R	Error register for hard drive 0 **Diagnostic mode** bits 7-3 = Reserved bits 2-0 = Errors 0001 No errors 0010 Controller error 0011 Sector buffer error 0100 ECC device error 0101 Control processor error **Operation mode** bit 7 = Block 0 Bad block 1 Block not bad bit 6 = Error 0 No error 1 Uncorrectable ECC error bit 5 = Reserved bit 4 = ID 0 ID located 1 ID not located bit 3 = Reserved bit 2 = Command 0 Completed 1 Not completed bit 1 = Track 000 0 Not found 1 Found bit 0 = DRAM 0 Not found 1 Found (CP-3022 always 0)
01F1h	W	Write precomposition register for hard drive 0
01F2h	R / W	Sector count for hard disk 0
01F3h	R / W	Sector number for hard drive 0
01F4h	R / W	Number of cylinders (low byte) for hard drive 0
01F5h	R / W	Number of cylinders (high byte) for hard drive 0

Continued...

I/O Address	Read/Write Status	Description
01F6h	R / W	Drive/Head register for hard drive 0 bit 7 = 1 bit 6 = 0 bit 5 = 1 bit 4 = Drive select 0 First hard drive 1 Second hard drive bits 3-0 = Head select bits
01F7h	R	Status register for hard drive 0 bit 7 = 1 Controller is executing a command bit 6 = 1 Drive is ready bit 5 = 1 Write fault bit 4 = 1 Seek operation complete bit 3 = 1 Sector buffer requires servicing bit 2 = 1 Disk data read completed successfully bit 1 = Index (is set to 1 at each disk revolution) bit 0 = 1 Previous command ended with error
01F7h	W	Command register for hard drive 0
0200h - 020Fh	R / W	Game controller ports
0201h	R / W	I/O data - game port
0220h – 022Fh	R / W	Soundport AD1816 reserved
I/O addresses 0278h - 027Ah are reserved for use with parallel port 2. See the bit definitions for addresses 0378h - 037Ah.		
0278h	R / W	Data port for parallel port 2
0279h	R	Status port for parallel port 2
0279h	W	PnP Address register (only for PnP devices)
027Ah	R / W	Control port for parallel port 2
02B0h – 02BFh	R / W	Digital I/O for Latch, WDOG, Control
I/O addresses 02E8h - 02EFh are reserved for use with serial port 4. See the bit definitions for I/O addresses 03F8h - 03FFh.		
02E8h	W	Transmitter holding register for serial port 4
02E8h	R	Receive buffer register for serial port 4
02E8h	R / W	Baud rate divisor (low byte) when DLAB = 1
02E9h	R / W	Baud rate divisor (high byte) when DLAB = 1
02E9h	R / W	Interrupt enable register when DLAB = 0
02EAh	R	Interrupt identification register for serial port 4
02EBh	R / W	Line control register for serial port 4
02ECh	R / W	Modem control register for serial port 4
02EDh	R	Line status register for serial port 4
02EEh	R	Modem status register for serial port 4
02EFh	R / W	Scratch register for serial port 4 (used for diagnostics)

Continued...

I/O Address	Read/Write Status	Description
I/O addresses 02F8h - 02FFh are reserved for use with serial port 2. See the bit definitions for I/O addresses 03F8h - 03FFh.		
02F8h	W	Transmitter holding register for serial port 2
02F8h	R	Receive buffer register for serial port 2
02F8h	R / W	Baud rate divisor (low byte) when DLAB = 1
02F9h	R / W	Baud rate divisor (high byte) when DLAB = 1
02F9h	R / W	Interrupt enable register when DLAB = 0
02FAh	R	Interrupt identification register for serial port 2
02FBh	R / W	Line control register for serial port 2
02FCh	R / W	Modem control register for serial port 2
02FDh	R	Line status register for serial port 2
02FEh	R	Modem status register for serial port 2
02FFh	R / W	Scratch register for serial port 2 (used for diagnostics)
0300h – 031Fh	R / W	LAN controller if installed
I/O addresses 0372h - 0377h are reserved for use with a secondary diskette controller. See the bit definitions for 03F2h - 03F7h.		
0372h	W	Digital output register for secondary diskette drive controller
0374h	R	Status register for secondary diskette drive controller
0375h	R / W	Data register for secondary diskette drive controller
0376h	R / W	Control register for secondary diskette drive controller
0377h	R	Digital input register for secondary diskette drive controller
0377h	W	Select register for secondary diskette data transfer rate
0378h	R / W	Data port for parallel port 1
0379h	R	Status port for parallel port 1 bit 7 = 0 Busy bit 6 = 0 Acknowledge bit 5 = 1 Out of paper bit 4 = 1 Printer is selected bit 3 = 0 Error bit 2 = 0 IRQ has occurred bit 1-0 = Reserved

Continued...

I/O Address	Read/Write Status	Description
037Ah	R / W	Control port for parallel port 1 bits 7-5 = Reserved bit 4 = 1 Enable IRQ bit 3 = 1 Select printer bit 2 = 0 Initialize printer bit 1 = 1 Automatic line feed bit 0 = 1 Strobe
03B0h - 03B8h	R / W	Various video registers
I/O addresses 03BCh - 03BEh are reserved for use with parallel port 3. See the bit definitions for addresses 0378h - 037Ah.		
03BCh	R / W	Data port - parallel port 3
03BDh	R / W	Status port - parallel port 3
03BEh	R / W	Control port - parallel port 3
03C0h - 03CFh	R / W	Video subsystem (EGA/VGA)
03C2h - 03D9h	R / W	Various CGA and CRTC registers
03E0h	R / W	PCCARD Address select
03E1h	R / W	PCCARD Data transfer with 365SL controller
I/O addresses 03E8h - 03EFh are reserved for use with serial port 3. See the bit definitions for I/O addresses 03F8h - 03FFh.		
03E8h	W	Transmitter holding register for serial port 3
03E8h	R	Receive buffer register for serial port 3
03E8h	R / W	Baud rate divisor (low byte) when DLAB = 1
03E9h	R / W	Baud rate divisor (high byte) when DLAB = 1
03E9h	R / W	Interrupt enable register when DLAB = 0
03EAh	R	Interrupt identification register for serial port 3
03EBh	R / W	Line control register for serial port 3
03ECh	R / W	Modem control register for serial port 3
03EDh	R	Line status register for serial port 3
03EEh	R	Modem status register for serial port 3
03EFh	R / W	Scratch register for serial port 3 (used for diagnostics)
03F2h	W	Digital output register for primary diskette drive controller bits 7-6 = 0 Reserved bit 5 = 1 Enable drive 1 motor bit 4 = 1 Enable drive 0 motor bit 3 = 1 Enable diskette DMA bit 2 = 0 Reset controller bit 1 = 0 Reserved bit 0 = 0 Select drive 0 1 Select drive 1

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I/O Address	Read/Write Status	Description
03F4h	R	Status register for primary diskette drive controller bit 7 = 1 Data register is ready bit 6 = 0 Transfer from system to controller 1 Transfer from controller to system bit 5 = 1 Non-DMA mode bit 4 = 1 Diskette drive controller is busy bits 3-2 = Reserved bit 1 = 1 Drive 1 is busy bit 0 = 1 Drive 0 is busy
03F5h	R / W	Data register for primary diskette drive controller
03F6h	R	Control port for primary diskette drive controller bits 7-4 = Reserved bit 3 = 0 Reduce write current 1 Head select enable bit 2 = 0 Disable diskette drive reset 1 Enable diskette drive reset bit 1 = 0 Disable diskette drive initialization 1 Enable diskette drive initialization bit 0 = Reserved
03F7h	R	Digital input register for primary diskette drive controller bit 7 = 1 Diskette drive line change bit 6 = 1 Write gate bit 5 = Head select 3 / reduced write current bit 4 = Head select 2 bit 3 = Head select 1 bit 2 = Head select 0 bit 1 = Drive 1 select bit 0 = Drive 0 select
03F7h	W	Select register for primary diskette data transfer rate bits 7-2 = Reserved bits 1-0 = 00 500 Kbs mode 01 300 Kbs mode 10 250 Kbs mode 11 Reserved
I/O addresses 03F8h - 03FFh are reserved for use with serial port 1. The bit definitions for these addresses also apply to serial ports 2, 3, and 4.		
03F8h	W	Transmitter holding register for serial port 1 - Contains the character to be sent. Bit 0, the least significant bit, is the first bit sent. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 0
03F8h	R	Receive buffer register for serial port 1 - Contains the character to be received. Bit 0, the least significant bit, is the first bit received. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 0

Continued...

I/O Address	Read/Write Status	Description
03F8h	R / W	Baud rate divisor (low byte) - This byte along with the high byte (03F9h) store the data transmission rate divisor. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 1
03F9h	R / W	Baud rate divisor (high byte) - This byte along with the low byte (03F8h) store the data transmission rate divisor. bits 7-0 = Bits 8-15 when DLAB = 1
03F9h	R / W	Interrupt enable register bits 7-4 = Reserved bit 3 = 1 Modem status interrupt enable bit 2 = 1 Receiver line status interrupt enable bit 1 = 1 Transmitter holding register empty interrupt enable bit 0 = 1 Received data available interrupt enable when DLAB = 0
03FAh	R	Interrupt identification register - serial port 1 bits 7-3 = Reserved bits 2-1 = Identify interrupt with highest priority 00 Modem status interrupt (4th priority) 01 Transmitter holding register empty (3rd priority) 10 Received data available (2nd priority) 11 Receiver line status interrupt (1st priority) bit 0 = 0 Interrupt pending (register contents can be used as a pointer to interrupt service routine) 1 No interrupt pending
03FBh	R / W	Line control register - serial port 1 bit 7 = Divisor Latch Access (DLAB) 0 Access receiver buffer, transmitter holding register, and interrupt enable register 1 Access divisor latch bit 6 = 1 Set break enable. Forces serial output to spacing state and remains there bit 5 = Stick parity bit 4 = Even parity select bit 3 = Parity enable bit 2 = Number of stop bits bit 1 = Word length 00 5-bit word length 01 6-bit word length 10 7-bit word length 11 8-bit word length
03FCh	R / W	Modem control register - serial port 1 bits 7-5 = Reserved bit 4 = 1 Loopback mode for diagnostic testing of serial port. bit 3 = 1 User-defined output 2 bit 2 = 1 User-defined output 1 bit 1 = Force Request To Send active bit 0 = Force Data Terminal Ready active

Continued...

I/O Address	Read/Write Status	Description
03FDh	R	Line status register - serial port 1 bit 7 = Reserved bit 6 = 1 Transmitting shift and holding registers empty bit 5 = 1 Transmitter shift register empty bit 4 = 1 Break interrupt bit 3 = 1 Framing error bit 2 = 1 Overrun error bit 0 = 1 Data ready
03FEh	R	Modem status register - serial port 1 bit 7 = 1 Data Carrier Detect bit 6 = 1 Ring Indicator bit 5 = 1 Data Set Ready bit 4 = 1 Clear To Send bit 3 = 1 Delta Data Carrier bit 2 = 1 Trailing Edge Ring Indicator bit 1 = 1 Delta Data Set Ready bit 0 = 1 Delta Clear To Send
03FFh	R / W	Scratch register - serial port 1 (used for diagnostics)
0A79h	W	PnP Data write register (only for PnP devices)

3.8 BIOS Data Area Definitions

The BIOS Data Area is an area within system RAM that contains information about the system environment. System environment information includes definitions associated with hard disks, diskette drives, keyboard, video, as well as other BIOS functions. This area is created when the system is first powered on. It occupies a 256-byte area from 0400h - 04FFh. The following table lists the contents of the BIOS data area locations in offset order starting from segment address 40:00h.

Location	Description
00h - 07h	I/O addresses for up to 4 serial ports
08h - 0Dh	I/O addresses for up to 3 parallel ports
0Eh - 0Fh	Segment address of extended data address
10h - 11h	Equipment list bits 15-14 = Number of parallel printer adapters 00 = Not installed 01 = One 10 = Two 11 = Three bits 13-12 = Reserved bits 11-9 = Number of serial adapters 00 = Not installed 001 = One 010 = Two 011 = Three 100 = Four bit 8 = Reserved bits 7-6 = Number of diskette drives 00 = One drive 01 = Two drives bits 5-4 = Initial video mode 00 = EGA or PGA 01 = 40 x 25 color 10 = 80 x 25 color 11 = 80 x 25 monochrome bit 3 = Reserved bit 2 = (1) Pointing device present bit 1 = (1) Math coprocessor present bit 0 = (1) Diskette drive present
12h	Reserved for port testing by manufacturer bits 7-1 = Reserved bit 0 = (0) Non-test mode (1) Test mode
13h	Memory size in kilobytes - low byte
14h	Memory size in kilobytes - high byte

Continued...

BIOS Data Area Definitions Continued...

Location	Description
15h - 16h	Reserved
17h	Keyboard Shift Qualifier States bit 7 = Insert mode bit 6 = CAPS lock bit 5 = Numlock bit 4 = Scroll Lock bit 3 = Either Alt key bit 2 = Either control key bit 1 = Left Shift key bit 0 = Right shift key 0 = not set / 1 = set
18h	Keyboard Toggle Key States bit 7 = (1) Insert held down bit 6 = (1) CAPS lock held down bit 5 = (1) Num Lock held down bit 4 = (1) Scroll Lock held down bit 3 = (1) Control+Num Lock held down bit 2 = (1) Sys Re held down bit 1 = (1) Left Alt held down bit 0 = (1) Left Control held down
19h	Scratch area for input from Alt key and numeric keypad
1Ah - 1Bh	Pointer to next character in keyboard buffer
1Ch - 1Dh	Pointer to last character in keyboard buffer
1Eh - 3Dh	Keyboard Buffer. Consists of 16 word entries.
3Eh	Diskette Drive Recalibration Flag bit 7 = (1) Diskette hardware interrupt occurred bits 6-4 = Not used bits 3-2 = Reserved bit 1 = (0) Recalibrate drive B bit 0 = (0) Recalibrate drive A

Continued...

BIOS Data Area Definitions Continued...

Location	Description
3Fh	Diskette Drive Motor Status bit 7 = Current operation 0 = Write or Format 1 = Read or Verify bit 6 = Reserved bits 5-4 = Drive Select 00 = Drive A 01 = Drive B bits 3-2 = Reserved 0 = Disable 1 = Enabled bit 1 = Drive B Motor Status 0 = Off 1 = On bit 1 = Drive A Motor Status 0 = Off 1 = On
40h	Diskette Drive Motor Timeout Disk drive motor is powered off when the value via the INT 08h timer interrupt reaches 0.
41h	Diskette Drive Status bit 7 = Drive Ready 0 = Ready 1 = Not ready bit 6 = Seek Error 0 = No error 1= Error occurred bit 5 = Controller operation 0 = Working 1 = Failed bits 4-0 = Error Codes 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 06h = Diskette change line active (door opened) 08h = DMA overrun error 09h = Data boundary error 0Ch = Unknown media type 10h = ECC or CRC error 20h = Controller failure 40h = Seek operation failure 80h = Timeout
42h - 48h	Diskette Controller Status Bytes
49h	Video Mode Setting
4Ah - 4Bh	Number of Columns on screen
4Ch - 4Dh	Size of Current Page, in bytes
4Eh - 4Fh	Address of Current Page

Continued...

BIOS Data Area Definitions Continued...

Location	Description
50h - 5Fh	Position of cursor for each video page. Current cursor position is stored two bytes per page. First byte specifies the column, the second byte specifies the row.
60h - 61h	Start and end lines for 6845-compatible cursor type. 60h = starting scan line, 61h = ending scan line.
62h	Current Video Display Page
63h - 64h	6845-compatible I/O port address for current mode 3B4h = Monochrome 3D4h = Color
65h	Register for current mode select
66h	Current palette setting
67 - 6Ah	Address of adapter ROM
6Bh	Last interrupt the occurred
6Ch - 6Dh	Low word of timer count
6Eh - 6Fh	High word of timer count
70h	Timer count for 24-hour rollover flag
71h	Break key flag
72h - 73h	Reset flag 1243h = Soft reset. Memory test is bypassed.
74h	Status of last hard disk operation 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 05h = Reset failed 08h = DMA overrun error 09h = Data boundary error 0Ah = Bad sector flag selected 0Bh = Bad track detected 0Dh = Invalid number of sectors on format 0Eh = Control data address mark detected 0Fh = DMA arbitration level out of range 10h = ECC or CRC error 11h = Data error corrected by ECC 20h = Controller failure 40h = Seek operation failure 80h = Timeout AAh = Drive not ready BBh = Undefined error occurred CCh = Write fault on selected drive E0h = Status error or error register = 0 FFh = Sense operation failed
75h	Number of hard drives
76h - 77h	Work area for hard disk

Continued...

BIOS Data Area Definitions Continued...

Location	Description
78h - 7Bh	Default parallel port timeout values
7Dh - 7Fh	Default serial port timeout values
80h - 81h	Pointer to start of keyboard buffer
82h - 83h	Pointer to end of keyboard buffer
84h - 88h	Reserved for EGA/VGA BIOS
8Ah	Reserved
8Bh	Diskette drive data transfer rate information bits 7-5 = Data rate on last operation 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bits 5-4 = Last drive step rate selected bits 3-2 = Data transfer rate at start of operation 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bits 1-0 = Reserved
8Ch	Copy of hard status register
8Dh	Copy of hard drive error register
8Eh	Hard drive interrupt flag
8Fh	Diskette controller information bit 7 = Reserved bit 6 = (1) Drive confirmed for drive B bit 5 = (1) Drive B is multi-rate bit 4 = (1) Drive B supports line change bit 3 = Reserved bit 2 = (1) Drive determined for drive A bit 1 = (1) Drive B is multi-rate bit 0 = (1) Drive B supports line change
90h - 91h	Media type for drives bits 7-6 = Data transfer rate 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bit 5 = (1) Double stepping required when 360K diskette inserted into 1.2MB drive bit 4 = (1) Known media is in drive bit 3 = Reserved bits 2-0 = Definitions upon return to user applications 000 = Testing 360K in 360K drive 001 = Testing 360K in 1.2 MB drive 010 = Testing 1.2 MB in 1.2 MB drive 011 = Confirmed 360K in 360K drive 100 = Confirmed 360K in 1.2 MB 101 = Confirmed 1.2 MB in 1.2 MB drive 111 = 720K in 720K drive or 1.44 MB in 1.44 MB drive

Continued...

BIOS Data Area Definitions Continued...

Location	Description
92h - 93h	Scratch area for diskette media. Low byte for drive A, high byte for drive B.
94h - 95h	Current track number for both drives. Low byte for drive A, high byte for drive B.
96h	Keyboard Status bit 7 = (1) Read ID bit 6 = (1) Last code was first ID bit 5 = (1) Force to Num Lock after read ID bit 4 = (1) Enhanced keyboard installed bit 3 = (1) Right ALT key active bit 2 = (1) Right Control key active bit 1 = (1) Last code was E0h bit 0 = (1) Last code was E1h
97h	Keyboard Status bit 7 = (1) Keyboard error bit 6 = (1) Updating LEDs bit 5 = (1) Resend code received bit 4 = (1) Acknowledge received bit 3 = Reserved bit 2 = (1) Caps lock LED state bit 1 = (1) Num lock LED state bit 0 = (1) Scroll lock LED state
98h - 99h	Offset address of user wait flag
9Ah - 9Bh	Segment address of user wait flag
9Ch - 9Dh	Wait count, in microseconds (low word)
9Eh - 9Fh	Wait count, in microseconds (high word)
A0h	Wait active flag bit 7 = (1) Time has elapsed bits 6-1 = Reserved bit 0 = (1) INT 15h, AH = 86h occurred
A1h - A7h	Reserved
A8h - ABh	Pointer to video parameters and overrides
ACh - FFh	Reserved
100h	Print screen status byte

3.8.1.1 Compatibility Service Table

In order to ensure compatibility with industry-standard memory locations for interrupt service routines and miscellaneous tabular data, the BIOS maintains tables and jump vectors.

Location	Description
FE05Bh	Entry Point for POST
FE2C3h	Entry point for INT 02h (NMI service routine)
FE3FEh	Entry point for INT 13h (Diskette Drive Services)
FE401h	Hard Drive Parameters Table
FE6F1h	Entry point for INT 19h (Bootstrap Loader routine)
FE6F5h	System Configuration Table
FE739h	Entry point for INT 14h (Serial Communications)
FE82Eh	Entry point for INT 16h (Keyboard Services)
FE897h	Entry point for INT 09h (Keyboard Services)
FEC59h	Entry point for INT 13h (Diskette Drive Services)
FEF57h	Entry point for INT OEh (Diskette Hardware Interrupt)
FEFC7h	Diskette Drive Parameters Table
FEFD2h	Entry point for INT 17h (Parallel Printer Services)
FF065h	Entry point for INT 10h (CGA Video Services)
FF0A4h	Video Parameter Table (6845 Data Table - CGA)
FF841h	Entry point for INT 12h (Memory Size Service)
FF84Dh	Entry point for INT 11h (Equipment List Service)
FF859h	Entry point for INT 15h (System Services)
Location	**Description**
FFA6Eh	Video graphics and text mode tables
FFE6Eh	Entry point for INT 1Ah (Time-of-Day Service)
FFEA5h	Entry Point for INT 08h (System Timer Service)
FFEF3h	Vector offset table loaded by POST
FFF53h	Dummy Interrupt routine IRET Instruction
FFF54h	Entry point for INT 05h (Print Screen Service)
FFFF0h	Entry point for Power-on
FFFF5h	BIOS Build Date (in ASCII)
FFFFEh	BIOS ID

3.9 VGA, LCD

3.9.1 VGA / LCD Controller 69000

69000 High Performance Flat Panel / CRT HiQVideo™ Accelerator with Integrated Memory

- Highly integrated Flat Panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, Clock Synthesizer, and integrated frame buffer
- Integrated High performance SDRAM memory. 2MB integrated memory, 83 MHz SDRAM operation
- HiQColor™ Technology implemented with TMED (Temporal Modulated Energy Distribution)
- Hardware Windows Acceleration
- Integrated composite NTSC / PAL Support
- Hardware Multimedia Support
- High-Performance Flat Panel Display resolution and color depth at 3.3V
- 36-bit direct interface to color and monochrom, single drive (SS), and dual drive (DD), STN & TFT panels
- Advanced Power Management features minimize power usage in:
  - Normal operation
  - Standby (Sleep) modes
  - Panel-Off Power-Saving Mode
- VESA Standards supported
- Fully Compatible with IBM® VGA
- Driver Support for Windows 3.1, Windows 95/98, Windows NT3.1/NT4.0

3.9.2 VGA / LCD BIOS for 69000

VGA BIOS

The 65555 and 69000 VGA BIOS (hereafter referred to as 69000 BIOS) is an enhanced, high performance BIOS that is used with the 69000 VGA Flat Panel/CRT Controller to provide an integrated Flat panel VGA solution. The BIOS is optimized for 69000 VGA Flat Panel/CRT Controller and provides:

Full compatibility with the IBM VGA BIOS
Support for monochrome LCD, 640x480, 800x600, 1024x768 and 1280x1024 TFT or STN displays.
Optional support for other displays.
Supports VESA BIOS Extensions, including VBE 2.0, VBE/DDC 1.0, and VBE/PM 1.0.
Supports either VESA local bus or PCI bus
Extended BIOS functions which offer easy access to 69000 control ler features and capabilities
Support for simultaneous display
44K BIOS supports 8 panels
48K BIOS supports 16 panels

High Performance Integrated Memory

The integrated SDRAM memory can support up to 83MHz operation, thus increasing the available memory bandwidth for the graphics subsystem. The result is support for additional high color / high resolution graphics modes combined with real-time video acceleration. This additional bandwidth also allows more flexibility in the other graphics functions intensely used in Graphics User Interface (GUIs) such as Microsoft™ Windows™.

Versatile Panel Support

The 69000 support a wide varety of monochrome and color Single-Panel, Single-Drive (SS) and Dual-Panel, Dual-Drive (DD), standard and high-resolution, passive STN and active matrix TFT/MIM LCD, and EL panels. With HiQColor™ technology, up to 256 gray scales are supported on passive STN LCDs. Up to 16.7M different colors can be displayed on passive STN LCDs and up to 16.7M colors on 24bit active matrix LCDs.

The 69000 offers a varety of programmable features to optimize display quality. Vertical centering and streching are provided for handling modes with less than 480 lines on 480-line panels. Horizontal and vertical streching capabilities are also available for both text and graphics modes for optimal display of VGA text and graphics modes on 800x600, 1024x768 and 1280x1024 panels.

Low Power Consumption

The 69000 uses a variety of advanced power management features to reduce power consumption of the display sub-system and to extend battery life. optimized for 3.3V operation, the 69000 internal logic, bus and panel interfaces operate at 3.3V but can tolerate 5V operation.

Software Compatibility / Flexibility

The 69000 is fully compatible with the VGA standard at both the register and BIOS levels. DIGITAL-LOGIC supply a fully VGA compatible BIOS, end-user utilities and drivers for common application programs.

Acceleration for All Panels and All Mode

The 69000 graphics engine is designed to support high performance graphics and video acceleration for all supported display resolutions, display types, and color modes. There is no compromise in performance operating in 8, 16, or 24 bpp color modes allowing true acceleration while displaying up to 16.7M colors.

3.9.3 Display Modes Supported

The 69000 supports the modes which appear in the table below.

Resolution	Color (bpp)	Refresh Rates (Hz)
640x480	8	60, 75, 85
640x480	16	60, 75, 85
640x480	24	60, 75, 85
800x600	8	60, 75, 85
800x600	16	60, 75, 85
800x600	24	60, 75, 85
1024x768	8	60, 75, 85
1024x768	16	60, 75, 85
1280x1024	8	60

3.9.4 VGA/LCD BIOS Support

Each LCD display needs a specific adapted VGA-BIOS.
This product is equipped with the CRT standard VGABIOS.

To connect a LCD display to this product, you need to perform the following:

1. Check the FP_LIST.PDF if the LCD BIOS is available.
   Get the latest VGA-BIOS at our webpage http://www.digitallogic.com

IF THE LCD BIOS IS AVAILABLE:

2. In the FLATPANEL-SUPPORT documentation the connection between the LCD and this product will be described.
3. DOWNLOAD the corresponding LCD-BIOS with the utility DOWN_000.EXE
   Go the the section 3.6 in this manual and follow those steps.
4. Restart the system and check the VGA-BIOS header message. The LCD name must be visible for only a short time. The VGABIOS message appears as first info page on the screen.
5. Stop the system, connect the LCD to the system and restart again
6. If on the LCD no image appears, as soon as the monitor begins to show the first text, stop the system immediately, otherways the LCD will get damaged.
7. Check the LCD connection again.

FOR A NEW LCD TYPE, NOT AVAILABLE NOW:

If the LCD BIOS for your LCD is not available, DIGITAL-LOGIC will adapt the LCD and provide you with one working cable. To initialise this, we need the following points from you:

1. An order to adapt the LCD (for the costs ask your sales contact)
2. Send the LCD panel, a datasheet, a connector to the LCD and the inverter for the backligth

ATTENTION:

DIGITAL-LOGIC AG is never responsible for a damaged LCD display. Even when there are mistakes in the BIOS or in any documentation for the LCD.

3.9.5 Memory 69000 CRT/TFT Panels

Hor. Resol.	Vert. Resol.	Color bpp	Refr. Hz	DCLK Mhz	MEM kByte	Cursor kByte	FB/C kByte	FB/M kByte	Video Input kByte	Total with Video	Total w/o Video
640	480	8	60	25.175	300	4.2	0	0	300	604	304
640	480	8	72	31.500	300	4.2	0	0	300	604	304
640	480	8	75	31.500	300	4.2	0	0	300	604	304
640	480	8	85	36.000	300	4.2	0	0	300	604	304
640	480	16	60	25.175	600	4.2	0	0	300	904	604
640	480	16	72	31.500	600	4.2	0	0	300	904	604
640	480	16	75	31.500	600	4.2	0	0	300	904	604
640	480	16	85	36.000	600	4.2	0	0	300	904	604
640	480	24	60	25.175	900	4.2	0	0	300	1204	904
640	480	24	72	31.500	900	4.2	0	0	300	1204	904
640	480	24	75	31.500	900	4.2	0	0	300	1204	904
640	480	24	85	36.000	900	4.2	0	0	300	1204	904
800	600	8	60	40.000	469	4.2	0	0	300	773	473
800	600	8	72	50.000	469	4.2	0	0	300	773	473
800	600	8	75	49.500	469	4.2	0	0	300	773	473
800	600	8	85	56.250	469	4.2	0	0	300	773	473
800	600	16	60	40.000	938	4.2	0	0	300	1242	942
800	600	16	72	50.000	938	4.2	0	0	300	1242	942
800	600	16	75	49.500	938	4.2	0	0	300	1242	942
800	600	16	85	56.250	938	4.2	0	0	300	1242	942
800	600	24	60	40.000	1406	4.2	0	0	300	1710	1410
800	600	24	72	50.000	1406	4.2	0	0	300	1710	1410
800	600	24	75	49.500	1406	4.2	0	0	300	1710	1410
800	600	24	85	56.250	1406	4.2	0	0	300	1710	1410
1024	768	16	60	65.000	1536	4.2	0	0	300	1840	1540
1024	768	16	70	75.000	1536	4.2	0	0	300	1840	1540
1024	768	16	75	78.750	1536	4.2	0	0	300	1840	1540
1024	768	16	85	94.500	1536	4.2	0	0	300	1840	1540
1024	768	24	60	65.000	2304	4.2	0	0	300	2608	2308
1024	768	24	72	75.000	2304	4.2	0	0	300	2608	2308
1024	768	24	75	78.750	2304	4.2	0	0	300	2608	2308
1024	768	24	85	94.500	2304	4.2	0	0	300	2608	2308
1280	1024	16	60	108.0	2560	4.2	0	0	300	2864	2564
1280	1024	16	70	128.0	2560	4.2	0	0	300	2864	2564
1280	1024	16	75	135.0	2560	4.2	0	0	300	2864	2564
1280	1024	16	85	157.5	2560	4.2	0	0	300	2864	2564
1280	1024	24	60	108.0	3840	4.2	0	0	300	4144!	3844
1280	1024	24	72	128.0	3840	4.2	0	0	300	4144!	3844
1280	1024	24	75	135.0	3840	4.2	0	0	300	4144!	3844
1280	1024	24	85	157.5	3840	4.2	0	0	300	4144!	3844

! means not possible resolution with the 4Mb Video RAM

3.9.6 Memory 69000 Color STN-DD Panels

Hor. Resol.	Vert. Resol.	Color bpp	Refr. Hz	DCLK Mhz	MEM kByte	Cursor kByte	FB/C kByte	FB/M kByte	Video Input kByte	Total with Video	Total w/o Video
640	480	8	60	25.175	300	4.2	120	0	300	724	424
640	480	8	72	31.500	300	4.2	120	0	300	724	424
640	480	8	75	31.500	300	4.2	120	0	300	724	424
640	480	8	85	36.000	300	4.2	120	0	300	724	424
640	480	16	60	25.175	600	4.2	120	0	300	1024	724
640	480	16	72	31.500	600	4.2	120	0	300	1024	724
640	480	16	75	31.500	600	4.2	120	0	300	1024	724
640	480	16	85	36.000	600	4.2	120	0	300	1024	724
640	480	24	60	25.175	900	4.2	120	0	300	1324	1024
640	480	24	72	31.500	900	4.2	120	0	300	1324	1024
640	480	24	75	31.500	900	4.2	120	0	300	1324	1024
640	480	24	85	36.000	900	4.2	120	0	300	1324	1024
800	600	8	60	40.000	469	4.2	188	0	300	960	660
800	600	8	72	50.000	469	4.2	188	0	300	960	660
800	600	8	75	49.500	469	4.2	188	0	300	960	660
800	600	8	85	56.250	469	4.2	188	0	300	960	660
800	600	16	60	40.000	938	4.2	188	0	300	1429	1129
800	600	16	72	50.000	938	4.2	188	0	300	1429	1129
800	600	16	75	49.500	938	4.2	188	0	300	1429	1129
800	600	16	85	56.250	938	4.2	188	0	300	1429	1129
800	600	24	60	40.000	1406	4.2	188	0	300	1898	1598
800	600	24	72	50.000	1406	4.2	188	0	300	1898	1598
800	600	24	75	49.500	1406	4.2	188	0	300	1898	1598
800	600	24	85	56.250	1406	4.2	188	0	300	1898	1598
1024	768	16	60	65.000	1536	4.2	307	0	300	2147	1847
1024	768	16	70	75.000	1536	4.2	307	0	300	2147	1847
1024	768	16	75	78.750	1536	4.2	307	0	300	2147	1847
1024	768	16	85	94.500	1536	4.2	307	0	300	2147	1847
1024	768	24	60	65.000	2304	4.2	307	0	300	2915	2615
1024	768	24	72	75.000	2304	4.2	307	0	300	2915	2615
1024	768	24	75	78.750	2304	4.2	307	0	300	2915	2615
1024	768	24	85	94.500	2304	4.2	307	0	300	2915	2615
1280	1024	16	60	108.0	2560	4.2	512	0	300	3376	3676
1280	1024	16	70	128.0	2560	4.2	512	0	300	3376	3676
1280	1024	16	75	135.0	2560	4.2	512	0	300	3376	3676
1280	1024	16	85	157.5	2560	4.2	512	0	300	3376	3676
1280	1024	24	60	108.0	3840	4.2	512	0	300	4656!	4356!
1280	1024	24	72	128.0	3840	4.2	512	0	300	4656!	4356!
1280	1024	24	75	135.0	3840	4.2	512	0	300	4656!	4356!
1280	1024	24	85	157.5	3840	4.2	512	0	300	4656!	4356!

! means not possible resolution with the 4Mb Video RAM

3.9.7 Memory 69000 Mono STN-DD Panels

Hor. Resol.	Vert. Resol.	Color bpp	Refr. Hz	DCLK Mhz	MEM kByte	Cursor kByte	FB/C kByte	FB/M kByte	Video Input kByte	Total with Video	Total w/o Video
640	480	8	60	25.175	300	4.2	0	38	300	642	342
640	480	8	72	31.500	300	4.2	0	38	300	642	342
640	480	8	75	31.500	300	4.2	0	38	300	642	342
640	480	8	85	36.000	300	4.2	0	38	300	642	342
640	480	16	60	25.175	600	4.2	0	38	300	942	642
640	480	16	72	31.500	600	4.2	0	38	300	942	642
640	480	16	75	31.500	600	4.2	0	38	300	942	642
640	480	16	85	36.000	600	4.2	0	38	300	942	642
640	480	24	60	25.175	900	4.2	0	38	300	1242	942
640	480	24	72	31.500	900	4.2	0	38	300	1242	942
640	480	24	75	31.500	900	4.2	0	38	300	1242	942
640	480	24	85	36.000	900	4.2	0	38	300	1242	942
800	600	8	60	40.000	469	4.2	0	59	300	832	532
800	600	8	72	50.000	469	4.2	0	59	300	832	532
800	600	8	75	49.500	469	4.2	0	59	300	832	532
800	600	8	85	56.250	469	4.2	0	59	300	832	532
800	600	16	60	40.000	938	4.2	0	59	300	1300	1000
800	600	16	72	50.000	938	4.2	0	59	300	1300	1000
800	600	16	75	49.500	938	4.2	0	59	300	1300	1000
800	600	16	85	56.250	938	4.2	0	59	300	1300	1000
800	600	24	60	40.000	1406	4.2	0	59	300	1769	1469
800	600	24	72	50.000	1406	4.2	0	59	300	1769	1469
800	600	24	75	49.500	1406	4.2	0	59	300	1769	1469
800	600	24	85	56.250	1406	4.2	0	59	300	1769	1469

! means not possible resolution with the 4Mb Video RAM

3.10 The Special Function Interface (SFI)

All functions are performed by starting the SW-interrupt 15h with the following arguments:

3.10.1 INT 15h SFR Functions

Function:	**WRITE TO EEPROM**
Number:	E0h
Description:	Writes the Data byte into the addressed User-Memory-Cell from the serial EEPROM. The old value is automatically deleted.
Input Values:	AH = E0h Function Request AL Databyte to store BX Address in the EEPROM (0-1024 Possible) SI 1234h User-Password (otherwise EEP is write-protected) DLAG-Password for access to the DLAG-Memory-Cells
Output Values:	None, all registers are preserved.

Function:	**READ FROM EEPROM**
Number:	E1h
Description:	Reads the Data byte from the addressed User-Memory-Cell of the serial EEPROM.
Input Values:	AH = E1h Function Request BX Address in the EEPROM (0-1024 Possible) SI 1234h User-Password DLAG-Password for access to the DLAG-Memory-Cells
Output Values:	AL read databyte

Function:	**WRITE SERIALNUMBER**
Number:	E2h
Description:	Writes the Serialnumber from the serial EEPROM into the addressed DLAG-Memory-Cell. The old value is automatically deleted.
Input Values:	AH = E2h Function Request DX,CX,BX Serialnumber (Binary, not Ascii) SI Password
Output Values:	None, all registers are preserved.

Function:	**READ SERIALNUMBER**
Number:	E3h
Description:	Reads the serialnumber from the board into the serial EEPROM.
Input Values:	AH = E3h Function Request
Output Values:	DX,CX,BX Serialnumber (Binary, not Ascii)

Function:	**WRITE PRODUCTION DATE & RESET DLAG-COUNTERS**
Number:	E4h
Description:	Writes the production date into the addressed DLAG-Memory-Cell from the serial EEPROM. The old value is automatically deleted. If the Password is also in DX, the counters will be resettet (=0).
Input Values:	AH = E4h Function Request BX Year (1997 => BH=19, BL=97) CH Month (1..12) CL Day of Month (1..31) SI Password DX Password, if counters should be resetted, otherwise no password.
Output Values:	None, all registers are preserved.

Function:	**READ PRODUCTION DATE**
Number:	E5h
Description:	Reads the production date from the board in the serial EEPROM.
Input Values:	AH = E5h Function Request
Output Values:	BX Year (1997 => BH=19, BL=97) CH Month (1..12) CL Day of Month (1..31)

Function:	**CHANGE VALUE IN KEYMATRIX**
Number:	E6h **NOT AVAILABLE ON THIS BOARD!**
Description:	Writes the data byte into the Keymatrix table from the EEPROM.
Input Values:	AH = E6h Function Request AL New Value to store in the table BX Address in the Keymatrix table in the EEPROM
Output Values:	None, all registers are preserved.

Function:	**TRANSFER KEYMATRIX TO EEPROM**
Number:	E7h **NOT AVAILABLE ON THIS BOARD!**
Description:	Transfers the Keymatrix table from the Keyboard controller to the serial EEPROM.
Input Values:	AH = E7h Function Request
Output Values:	None, all registers are preserved.

Function:	**WRITE INFO2 TO THE EEPROM**
Number:	F0h (PHOENIX) E8h (AMI)
Description:	Writes the information bytes into the serial EEPROM.
Input Values:	AH = F0h Function Request (PHOENIX) AH = E8h Function Request (AMI) AL Board Type (M= PC/104, E=Euro, W=MSWS, S=Slot, C=Custom) DI CPU Type (1=ELAN310, 2=ELAN400, 3=486SLC, 4=486DX, 5=P5) BX Board Version (Ex: V1.5 => BH=1, BL=5) CX BIOS Version (Ex: V3.0 => CH=3, CL=0) DH Number of 512k Flash DL Number of 512k SRAM SI Password
Output Values:	None, all registers are preserved.

Function:	**READ INFO2 FROM THE EEPROM**
Number:	E9h
Description:	Reads the information bytes out of the serial EEPROM.
Input Values:	AH = E9h Function Request
Output Values:	AL Board Type (M= PC/104, E=Euro, W=MSWS, S=Slot, C=Custom) DI CPU Type (1=ELAN310, 2=ELAN400, 3=486SLC, 4=486DX, 5=P5) BX Board Version (Ex: V1.5 => BH=1, BL=5) CX BIOS Version (Ex: V3.0 => CH=3, CL=0) DH Number of 512k Flash DL Number of 512k SRAM

Function:	**READ INFO3 FROM THE EEPROM**
Number:	EAh
Description:	Reads the information bytes out of the serial EEPROM.
Input Values:	AH = EAh Function Request
Output Values:	AX counter of BOOTERRORS counter of SETUP ENTRIES counter of LOW BATTERY ERROR counter of BOOT UP SYSTEM

Function:	**WATCHDOG**
Number:	EBh
Description:	Enables, strobes and disables the WATCHDOG. After power-up, the Watchdog is always disabled. Once the Watchdog has been enabled, the user application must perform a strobe at least every 800ms, other- wise the watchdog performs a hardware reset.
Input Values:	AH = EBh Function Request AL 00 Disable Watchdog 01..FE Enable Watchdog FF Strobe Watchdog
Output Values:	None, all registers are preserved.

Function:	**READ TEMPERATURE OF LM75**
Number:	ECh
Description:	Reads the temperature from the LM75.
Input Values:	AH = ECh Function Request
Output Values:	AL temperature BL 00 =>value OK, otherwise NOK

Function: **SET POWERSAVE**

Number: EDh

Description: Sets Powersave options.

Input Values: AH = EDh Function Request
AL 00 => LCD Powersave
BL Bit 2
LCD-VDD on/off NOT AVAILABLE
Bit 1
LCD-VEE on/off NOT AVAILABLE
Bit 0
LCD-Backl. on/off NOT AVAILABLE

01 => HD0 Powersave
AVAILABLE
BL 0
The drive will immediately go to the Standby mode.
1 The drive will immediately go to the active mode.
2 The drive will immediately go to the standby mode.
If the sector count registers is zero then the timer will be disabled.
If the sector count register is non-zero the timer will be enabled and initialized with the sector count value.
3 The drive will immediately go to the active mode.If the sector count registers is zero then the timer will be disabled. If the sector count register is non-zero the timer will be enabled and initialized with the sector count value.
5 If the drive is in active mode, the sector count registers will be set to 0FFh. If the drive is in, going to, or recovering from the standby mode, the sector count register will be set to 000h.
6 The drive enters the sleep mode. Either a soft- or hardware reset is required to recover from this mode. The drive will then go to the standby mode.

02 => HD1 Powersave
BL Same as HD0 Powersave

Output Values: None, all registers are preserved

Function:	**LED SWITCH-STATUS**	
Number:	EEh	
NOT AVAILABLE ON THIS BOARD!		
Description:	Sets LED and reads the switches.	
Input Values:	AH = EEh	Function Request
	AL	01 Set LEDs only 02 Reads Switches only 03 Set LEDs and read Switches
	BL	Only for Set LED mode used LEDs Bit X is LED X
Output Values:	AL	Switches, if mode is set, otherwise all registers are preserved.

Function:	**INFORMATION ABOUT INT15-SUPPORT ON THE BOARD**	
Number:	EEh	
Description:	Gives informations about the supported interrupt 15 functions.	
Input Values:	AH = EFh	Function Request
	AL	Number of Interrupt, where you need information
	SI	Password, if you want information about a password saved Interrupt
Output Values:	BX	Interrupt-Information Word
	BH	Version number of Interrupt (0 = not supported) If there is a Password-saved Interrupt, a zero is shown, if the password is wrong.
	BL	Second-Version number.

3.11 Remote function (PHOENIX)

Use a Null- modem cable to connect COM1 of the DLAG- board to COM1 (COM2) port of the host- PC. These are the minimum requirements:

	D-Sub 1	D-Sub 2	
Receive Data	2	3	Transmit Data
Transmit Data	3	2	Receive Data
Data Terminal Ready	4	6	Data Set Ready
System Ground	5	5	System Ground
Request to Send	7	8	Clear to Send

When the option REMOTE is enabled in the BIOS, start the program HOSTKEY.EXE on the host- PC. After that, start the DLAG board and one will see the context on the host – PC.

Usage: HOSTKEY [/? | /Cx | /Sxx | /NOF | /V]

where /? = this screen
/C1 = COM1 (DEFAULT)
/C2 = COM2
/S96 = 9600 baud
/S192 = 19200 baud
/S384 = 38400 baud
/S576 = 57600 baud
/S1152 = 115200 baud (DEFAULT)
/NOF = do not check for floopy disk when loading HOSTKEY
/V = verbose mode, display HOSTKEY messages

Example:
HOSTKEY /C1 /S384 /V

Control-X to exit. **CTRL-ALT-F10** to reboot target.

NOTE:
- Chipset BX has **no** USB support while in REMOTE mode
- Chipset TX has USB support while in REMOTE mode

3.12 WatchDOG Control

Interface/Function:	On smartModule:	Needed circuits on OEM board:
External WatchDOG Control	Standard automatically strobed with 32kHz	Pin B108 or B109 must be controlled, if the watchdog function should work.

- The WatchDOG in the smartModule-P5PC is connected over a free running 32kHz oscillator. This prevents to restart the system, if no external circuit at pin B108 or B109 is connected.
  These pins are OR-wired with the internally strobed clock.

- When pin B108 or B109 are open (not connected), the WatchDOG is strobed at fulltime, that means, that the system is free running and no restart may overcome.

- When pin B108 or B109 are set to GND, the watchDOG is no longer strobed.
  After approx. 800ms, the system restarts automatically.

4 DESCRIPTION OF THE JUMPERS

The jumpers

	CPU speed selection	J86 BF0	J87 BF1	J88 BF2
166Mhz	Factory settings	1-2	1-2	1-2
266Mhz	**Factory settings**	**1-2**	**1-2**	**2-3**
266Mhz	266Mhz CPU reduced to 166Mhz	1-2	1-2	1-2

Jumper	Texture	1-2 = open	2-3 = closed
J07	CPU CLK	100 MHz (not supported)	**66 MHz**
J114	BIOS CHIPSELECT programming	EXTERNAL	**INTERNAL**

Settings written in bold are defaults!

4.1 The jumpers on the SM586PC

5 LED CRITERIONS:

LED	Color	Function
D26	Green	Run OK
D31	Green	3.3 V OK
D33	Red	LAN ACTIVE (until V2.0)

5.1 2 Power / control LEDs on the SM586PC

On the topside of the smartModule-586PC are 2 LED's located.

1. **The GREEN POWER LED**

   Indicates, that the 3.3V core supply for the CPU is OK.
   This LED must light, as soon as the external 5V power supply is available.

2. **The GREEN RESET/RUN LED**

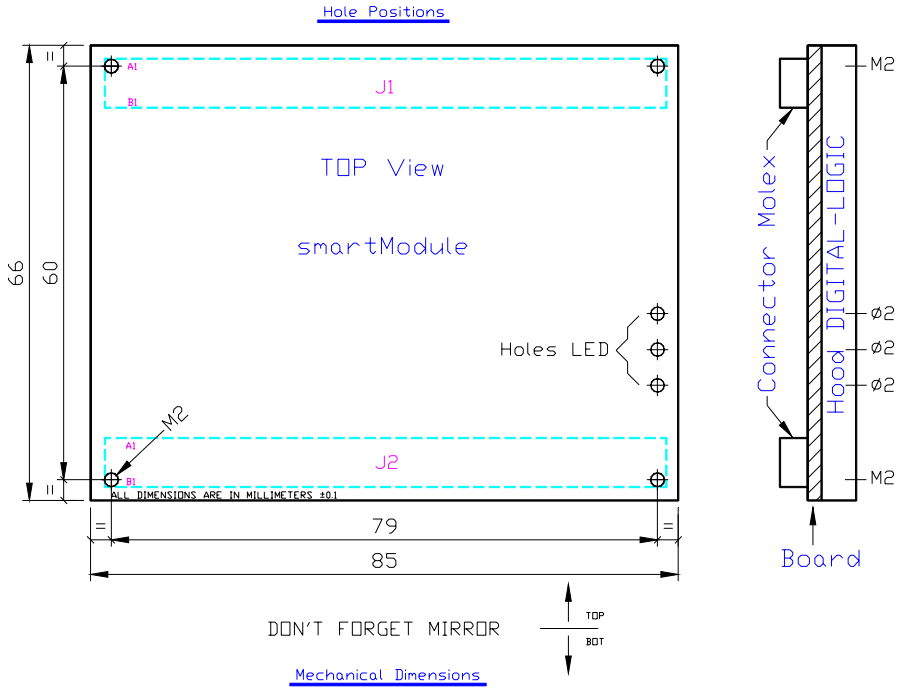
   OFF: The module is in the RESET state, that means, no operation.
   The WatchDOG or the power supervisor or an active external reset signal holds the modul in the RESET state.

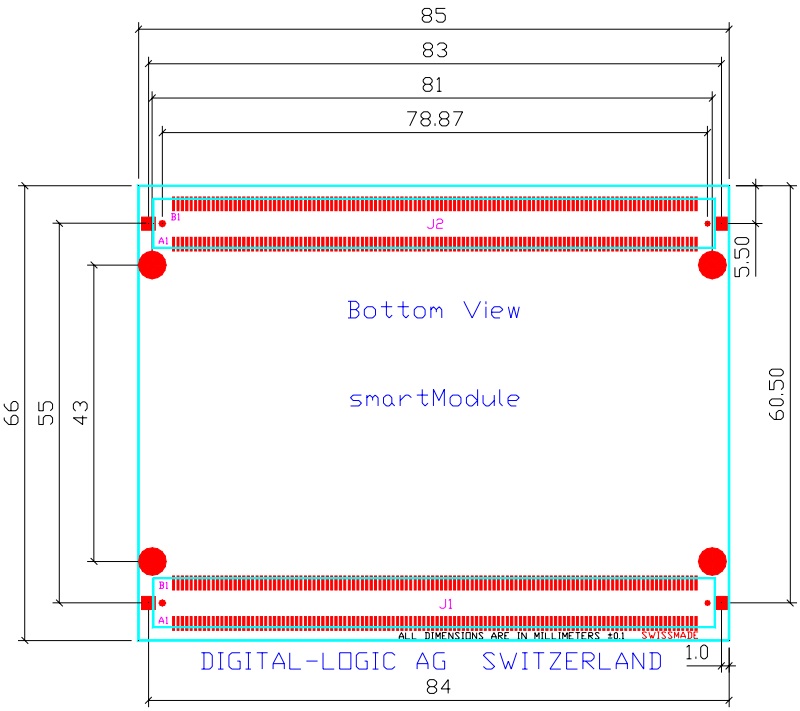
   ON: The module is running normally.
   After power up, this LED must light ON after 1-2sec.

AFTER A SUCCESSFUL BOOT SEQUENCE: TWO GREEN LED'S ARE ON!

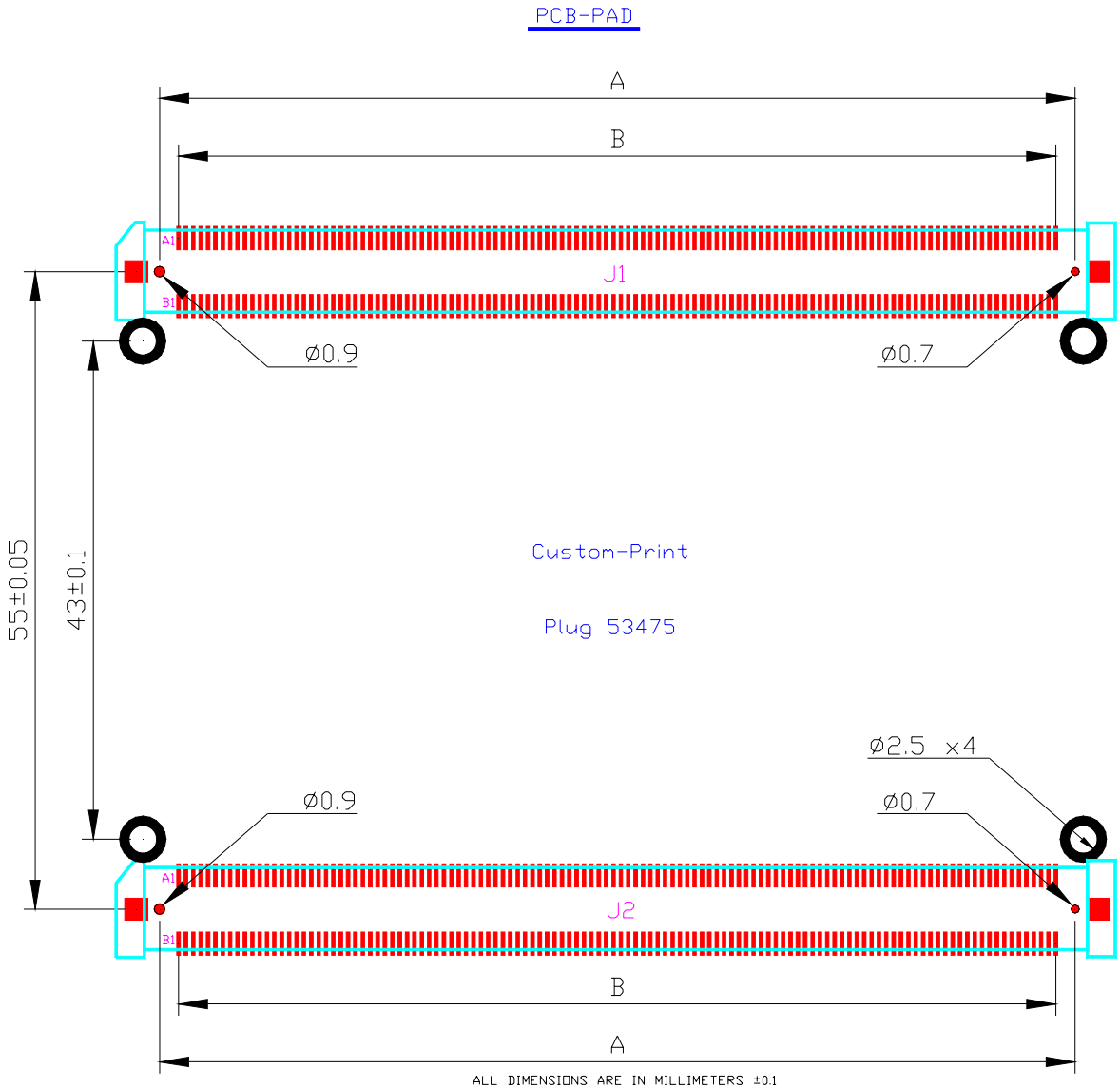
6 DESIGNIN WITH THE smartModule

6.1 Mechanical Dimensions SM586PC





6.1.1 Mechanical PCB Pad Dimensions on the Carrier-Board



Customer board

53475-2409 Circuits	Dimension mm (inches)	
	A	B
240	78.07 (3.070)	75.565 (2.970)

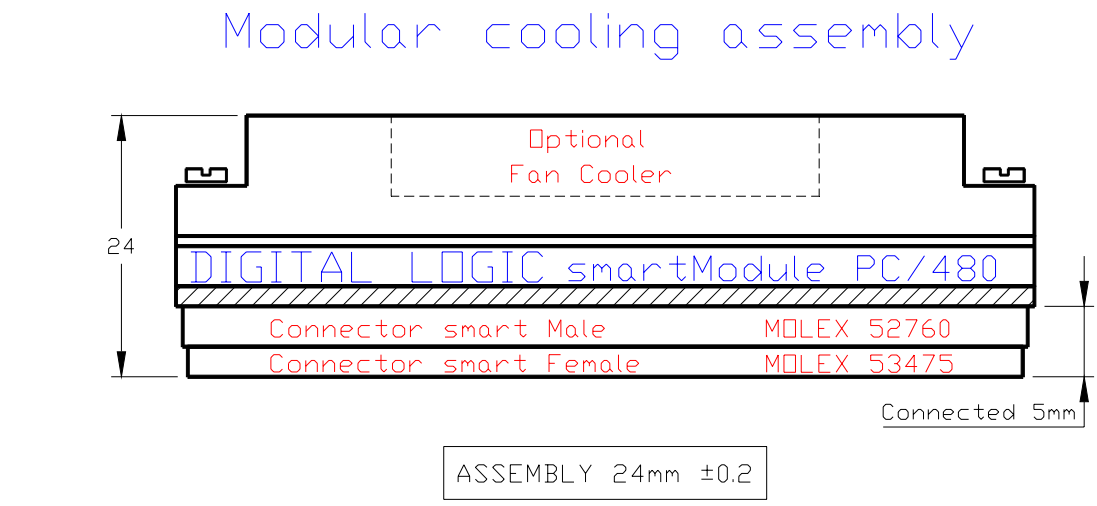
DIGITAL-LOGIC / Art_Nr : 439004 Connected: 5.00mm

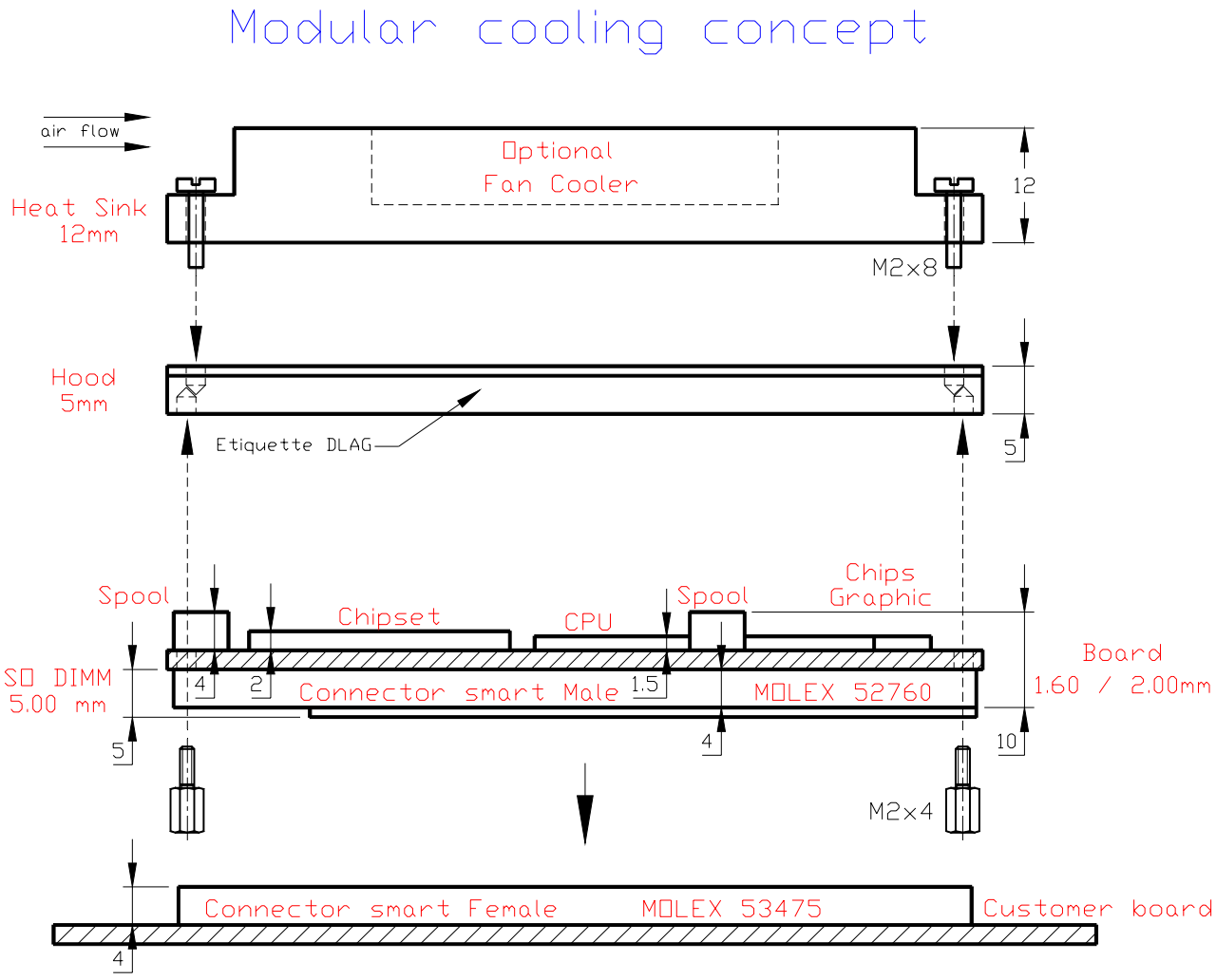
smartModule

52760-2409 Circuits	Dimension mm (inches)	
	A	B
240	78.87 (3.105)	75.565 (2.970)

DIGITAL-LOGIC / Art_Nr : 439003 Receptable

6.1.2 PCB to SM586PC height

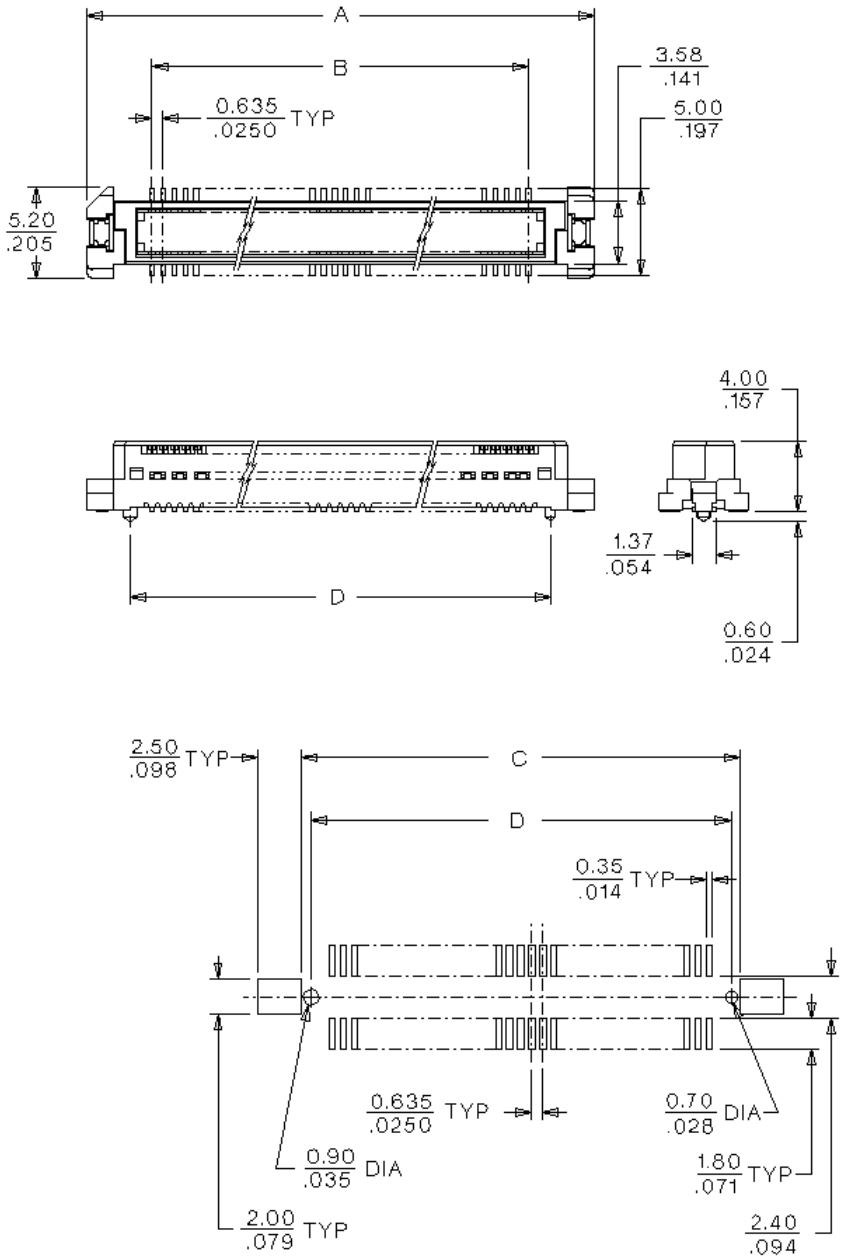




6.1.3 Mechanical Dimensions of the PCB, plug

Must be mounted onto the customers electronicboard (carrierboard).

Standard height: 5.0mm (do not place components below the smartModule)
Expanded height: 7.0mm (place max. 2.0mm components below the smartModule)



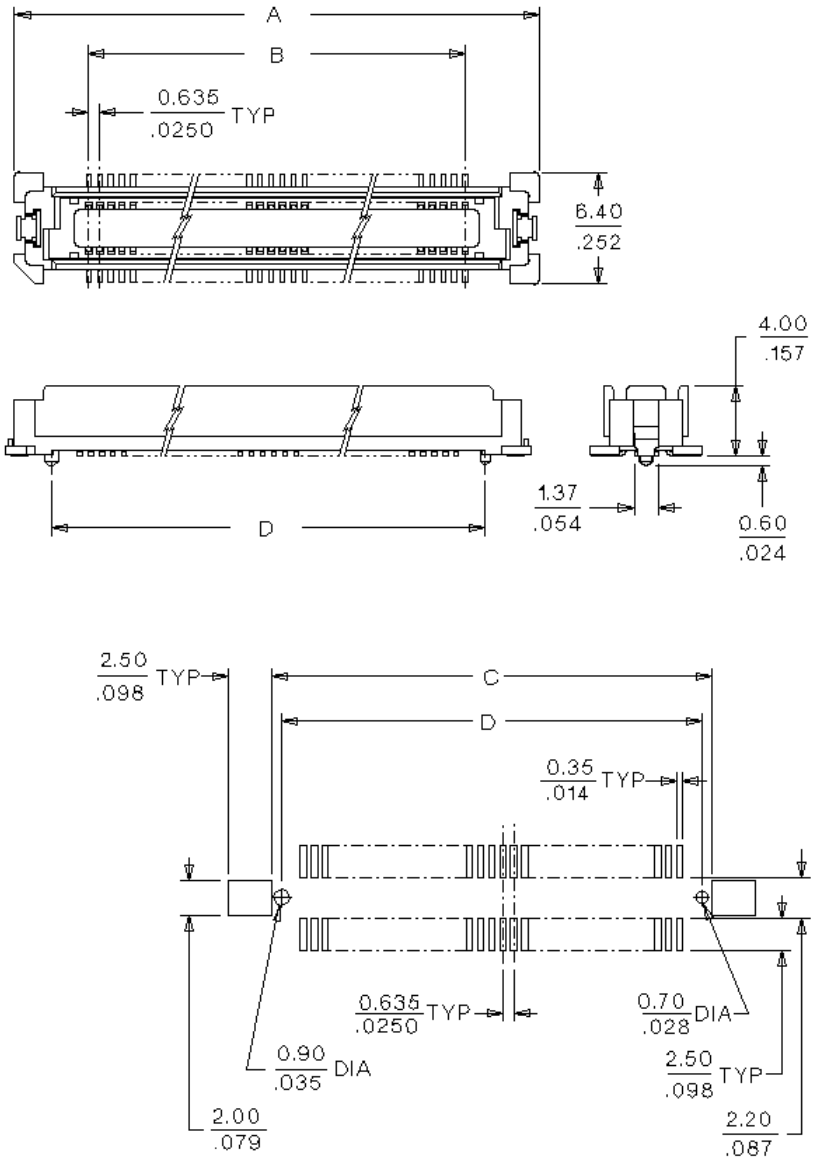
PCB LAYOUT : COMPONENT SIDE

53475-2409 Circuits	Dimension **mm** (inches)			
	A (Overall Length)	**B (1st to Last Ckt)**	**C**	**D**
240	**83.07**(3.270)	**75.565**(2.970)	**79.17**(3.110)	**78.07**(3.070)

DLAG partnumber: 439004

6.1.4 Mechanical Dimensions of the SM586PC, receptacle

Mounted on the smartModule 586PC, as a reference only



PCB LAYOUT: COMPONENT SIDE

52760-2409 **Circuits**	Dimension **mm** (inches)			
	A	**B**	**C**	**D**
240	**84.07(3.309)**	**75.565(2.970)**	**80.47(3.168)**	**78.87(3.105)**

DLAG part number: 439003

6.2 The generic smart480 bus

6.2.1 (sinceVers. 2.1)

SM586PC Connector J1 Pin 1-40

Pin	Group	Volt	SM586PC	Pin	Group	Volt	SM586PC
A1	POWER		VCC (5V)	B1	ISA	5 i	IRQ1
A2	ISA	5 o	RESDRV	B2	ISA	5 i	IRQ5
A3	ISA	5 i	SBHE#	B3	ISA	5 i	IRQ3
A4	ISA	5 i	MEMCS16#	B4	ISA	5 i	IRQ4
A5	ISA	5 i	IOCS16#	B5	ISA	5 i	IRQ5
A6	ISA	5 o	IOW#	B6	ISA	5 i	IRQ6
A7	ISA	5 o	IOR#	B7	ISA	5 i	IRQ7
A8	ISA	5 o	SYSCLK	B8	ISA	5 i	IRQ10
A9	ISA	5 o	TC	B9	ISA	5 i	IRQ11
A10	ISA	5 o	ALE	B10	ISA	5 i	IRQ12
A11	ISA	5 i/o	SD7	B11	ISA	5 i	IRQ14
A12	ISA	5 i/o	SD6	B12	ISA	5 i	IRQ15
A13	ISA	5 i/o	SD5	B13	CORE	5 i	COREBIOS Enable
A14	ISA	5 i/o	SD4	B14	CORE	5 i	VGABIOS Enable
A15	ISA	5 i/o	SD3	B15	ISA	5 o	LA21
A16	ISA	5 i/o	SD2	B16	ISA	5 o	LA20
A17	ISA	5 i/o	SD1	B17	ISA	5 o	LA19
A18	ISA	5 i/o	SD0	B18	ISA	5 o	LA18
A19	ISA	5 o	IOCHRDY	B19	ISA	5 o	LA17
A20	ISA	5 o	AEN	B20	ISA	5 i/o	SD8
A21	ISA	5 o	SA19	B21	ISA	5 i/o	SD9
A22	ISA	5 o	SA18	B22	ISA	5 i/o	SD10
A23	ISA	5 o	SA17	B23	ISA	5 i/o	SD11
A24	ISA	5 o	SA16	B24	ISA	5 i/o	SD12
A25	ISA	5 o	SA15	B25	ISA	5 i/o	SD13
A26	ISA	5 o	SA14	B26	ISA	5 i/o	SD14
A27	ISA	5 o	SA13	B27	ISA	5 i/o	SD15
A28	ISA	5 o	SA12	B28	ISA	5 i	DRQ 0
A29	ISA	5 o	SA11	B29	ISA	5 i	DRQ 1
A30	ISA	5 o	SA10	B30	ISA	5 i	DRQ 2
A31	ISA	5 o	SA9	B31	ISA	5 i	DRQ 3
A32	ISA	5 o	SA8	B32	ISA	5 i	DRQ 5
A33	ISA	5 o	SA7	B33	ISA	5 i	DRQ 6
A34	ISA	5 o	SA6	B34	ISA	5 o	OSC (14.31MHz)
A35	ISA	5 o	SA5	B35	ISA	5 o	DMA0#
A36	ISA	5 o	SA4	B36	ISA	5 o	DMA1#
A37	ISA	5 o	SA3	B37	ISA	5 o	DMA2#
A38	ISA	5 o	SA2	B38	ISA	5 o	DMA3#
A39	ISA	5 o	SA1	B39	ISA	5 o	DMA5#
A40	ISA	5 o	SA0	B40	ISA	5 o	DMA6#

** These signals (LA17-LA19) correspond with the SA17-SA19.

Remarks:

5 o = 5V output 5 i/o = 5V input/output
3 o = 3V output 3 i/o = 3V input/output

# = active low signal o.c. = open collector output NC = not connected
RES = pin function depending of the CPU, reserved

SM586PC Connector J1 Pin 41-80 (Vers. 2.1)

Pin	Group	Volt	SM586PC	Pin	Group	Volt	SM586PC
A41	DRAM	3 o	CAS0-	B41	CORE	5 o	Speaker
A42	DRAM	3 o	CAS1-	B42	ISA	5 i	ZWS#
A43	DRAM	3 o	CAS2-	B43	ISA	5 o	REF#
A44	DRAM	3 o	CAS3-	B44	ISA	5 o	MEMR#
A45	DRAM	3 o	CAS4-	B45	ISA	5 o	SMEMR#
A46	DRAM	3 o	CAS5-	B46	ISA	5 o	MEMW#
A47	DRAM	3 o	CAS6-	B47	ISA	5 o	SMEMW#
A48	DRAM	3 o	CAS7-	B48	IDE-CH2	5 i/o	IDE HD 0
A49	DRAM	3 i/o	MD0	B49	IDE-CH2	5 i/o	IDE HD 1
A50	DRAM	3 i/o	MD1	B50	IDE-CH2	5 i/o	IDE HD 2
A51	DRAM	3 i/o	MD2	B51	IDE-CH2	5 i/o	IDE HD 3
A52	DRAM	3 i/o	MD3	B52	IDE-CH2	5 i/o	IDE HD 4
A53	DRAM	3 i/o	MD4	B53	IDE-CH2	5 i/o	IDE HD 5
A54	DRAM	3 i/o	MD5	B54	IDE-CH2	5 i/o	IDE HD 6
A55	DRAM	3 i/o	MD6	B55	IDE-CH2	5 i/o	IDE HD 7
A56	DRAM	3 i/o	MD7	B56	IDE-CH2	5 i/o	IDE HD 8
A57	POWER		GROUND	B57	IDE-CH2	5 i/o	IDE HD 9
A58	DRAM	3 i/o	MD8	B58	IDE-CH2	5 i/o	IDE HD 10
A59	DRAM	3 i/o	MD9	B59	IDE-CH2	5 i/o	IDE HD 11
A60	DRAM	3 i/o	MD10	B60	IDE-CH2	5 i/o	IDE HD 12
A61	DRAM	3 i/o	MD11	B61	IDE-CH2	5 i/o	IDE HD 13
A62	DRAM	3 i/o	MD12	B62	IDE-CH2	5 i/o	IDE HD 14
A63	DRAM	3 i/o	MD13	B63	IDE-CH2	5 i/o	IDE HD 15
A64	DRAM	3 i/o	MD14	B64	IDE-CH2	5 o	IDE cs0#
A65	DRAM	3 i/o	MD15	B65	IDE-CH2	5 o	IDE cs1#
A66	POWER		GROUND	B66	IDE-CH2	5 o	IDE IOR
A67	DRAM	3 i/o	MD16	B67	IDE-CH2	5 o	IDE IOW
A68	DRAM	3 i/o	MD17	B68	DRAM	5 o	S DCLK2
A69	DRAM	3 i/o	MD18	B69	NC		NC
A70	DRAM	3 i/o	MD19	B70	NC		NC
A71	DRAM	3 i/o	MD20	B71	DRAM	5 o	S CASA
A72	DRAM	3 i/o	MD21	B72	DRAM	5 o	S CASB
A73	DRAM	3 i/o	MD22	B73	DRAM	5 o	S RASA
A74	DRAM	3 i/o	MD23	B74	DRAM	5 o	S CASB
A75	DRAM	3 o	MA0	B75	DRAM	5 o	RAS4 (TX)
A76	DRAM	3 o	MA1	B76	DRAM	5 o	RAS5 (TX)
A77	DRAM	3 o	MA2	B77	DRAM	5 o	MA13
A78	DRAM	3 o	MA3	B78	DRAM	5 o	S DCLK0
A79	DRAM	3 o	MA4	B79	DRAM	5 o	S DCLK1
A80	DRAM	3 o	MA5	B80	CORE	3 o	24MHz Output

Remarks:

5 o = 5V output 5 i/o = 5V input/output
3 o = 3V output 3 i/o = 3V input/output

# = active low signal o.c. = open collector output NC = not connected
RES = pin function depending of the CPU, reserved

P5 CPU with 64Bit Memorybus:
CASL0-CASL3 Bank 0,2 CAS0 .... CAS7 to all banks
CASH0-CASH3 Bank 1,3

SM586PC Connector J1 Pin 81-120 (Vers. 2.1)

Pin	Group	Volt	SM586PC	Pin	Group	Volt	SM586PC
A81	DRAM	3 o	MA 6	B81	POWER		Ground
A82	DRAM	3 o	MA 7	B82	DRAM	3 i/o	MD48
A83	DRAM	3 o	MA 8	B83	DRAM	3 i/o	MD49
A84	DRAM	3 o	MA 9	B84	DRAM	3 i/o	MD50
A85	DRAM	3 o	MA 10	B85	DRAM	3 i/o	MD51
A86	DRAM	3 o	MA 11	B86	DRAM	3 i/o	MD52
A87	DRAM	3 o	MA 12	B87	DRAM	3 i/o	MD53
A88	POWER		Ground	B88	DRAM	3 i/o	MD54
A89	DRAM	3 i/o	MD24	B89	DRAM	3 i/o	MD55
A90	DRAM	3 i/o	MD25	B90	POWER		GROUND
A91	DRAM	3 i/o	MD26	B91	DRAM	3 i/o	MD56
A92	DRAM	3 i/o	MD27	B92	DRAM	3 i/o	MD57
A93	DRAM	3 i/o	MD28	B93	DRAM	3 i/o	MD58
A94	DRAM	3 i/o	MD29	B94	DRAM	3 i/o	MD59
A95	DRAM	3 i/o	MD30	B95	DRAM	3 i/o	MD60
A96	DRAM	3 i/o	MD31	B96	DRAM	3 i/o	MD61
A97	POWER		GROUND	B97	DRAM	3 i/o	MD62
A98	DRAM	3 i/o	MD32	B98	DRAM	3 i/o	MD63
A99	DRAM	3 i/o	MD33	B99	POWER		GROUND
A100	DRAM	3 i/o	MD34	B100	IDE-CH2	5 i/o	SDACK
A101	DRAM	3 i/o	MD35	B101	IDE-CH2	5 i/o	SDRQ
A102	DRAM	3 i/o	MD36	B102	IDE-CH2	5 i/o	IRQ
A103	DRAM	3 i/o	MD37	B103	IDE-CH2	5 i/o	SIORDY
A104	DRAM	3 i/o	MD38	B104	IDE-CH2	5 i/o	A0
A105	DRAM	3 i/o	MD39	B105	IDE-CH2	5 i/o	A1
A106	POWER		GROUND	B106	IDE-CH2	5 i/o	A2
A107	DRAM	3 i/o	MD40	B107	DRAM	3 o	BA0
A108	DRAM	3 i/o	MD41	B108	Core	5 i#	WDOG Strobe
A109	DRAM	3 i/o	MD42	B109	Core	5 i#	WDOG Strobe
A110	DRAM	3 i/o	MD43	B110	DRAM	3 o	BA1
A111	DRAM	3 i/o	MD44	B111	XBUS	3 o	XD0
A112	DRAM	3 i/o	MD45	B112	XBUS	3 o	XD1
A113	DRAM	3 i/o	MD46	B113	XBUS	3 o	XD2
A114	DRAM	3 i/o	MD47	B114	XBUS	3 o	XD3
A115	DRAM	3 o	RAS0#	B115	XBUS	3 o	XD4
A116	DRAM	3 o	RAS1#	B116	XBUS	3 o	XD5
A117	DRAM	3 o	RAS2#	B117	XBUS	3 o	XD6
A118	DRAM	3 o	RAS3#	B118	XBUS	3 o	XD7
A119	DRAM	3 o	MWEA#	B119	ISA	3 o	BIOSCS
A120	DRAM	3 o	MWEB#	B120	POWER		VCC (5 Volt)

Remarks:

5 o = 5V output 5 i/o = 5V input/output
3 o = 3V output 3 i/o = 3V input/output

# = active low signal o.c. = open collector output NC = not connected
RES = pin function depending of the CPU, reserved

Memorybus width: 586: 64Bit (MD0 – MD63))

SM586PC Connector J2 Pin 1-40 (Vers. 2.1)

Pin	Group	Volt	SM586PC	Pin	Group	Volt	SM586PC
A1	PRINTER	5 o	strobe#	B1	COM1	5 o	DCD1
A2	PRINTER	5 o	auto#	B2	COM1	5 i	DSR1
A3	PRINTER	5 o	error#	B3	COM1	5 i	RXD1
A4	PRINTER	5 o	init#	B4	COM1	5 o	RTS1
A5	PRINTER	5 o	slctin#	B5	COM1	5 o	TXD1
A6	PRINTER	5 i/o	PRINTER data 0	B6	COM1	5 i	CTS1
A7	PRINTER	5 i/o	PRINTER data 1	B7	COM1	5 o	DTR1
A8	PRINTER	5 i/o	PRINTER data 2	B8	COM1	5 i	RI1
A9	PRINTER	5 i/o	PRINTER data 3	B9	COM2	5 o	DCD2
A10	PRINTER	5 i/o	PRINTER data 4	B10	COM2	5 i	DSR2
A11	PRINTER	5 i/o	PRINTER data 5	B11	COM2	5 i	RXD2
A12	PRINTER	5 i/o	PRINTER data 6	B12	COM2	5 o	RTS2
A13	PRINTER	5 i/o	PRINTER data 7	B13	COM2	5 o	TXD2
A14	PRINTER	5 i	acknowledge#	B14	COM2	5 i	CTS2
A15	PRINTER	5 i	busy	B15	COM2	5 o	DTR2
A16	PRINTER	5 i	paper end	B16	COM2	5 i	RI2
A17	PRINTER	5 i	select	B17	FLOPPY	5 i	index
A18	KBD	5 i/o	keyboard data	B18	FLOPPY	5 o	drive select 1
A19	KBD	5 o	keyboard clock	B19	FLOPPY	5 i	disk change
A20	MOUSE	5 o	MOUSE clock	B20	FLOPPY	5 o	motor on 1
A21	MOUSE	5 i/o	MOUSE data	B21	FLOPPY	5 o	direction
A22	POWER		Ground	B22	FLOPPY	5 o	step impulse
A23	IDE-CH1	5 i/o	IDE HD 0	B23	FLOPPY	5 o	write data
A24	IDE-CH1	5 i/o	IDE HD 1	B24	FLOPPY	5 o	write gate
A25	IDE-CH1	5 i/o	IDE HD 2	B25	FLOPPY	5 i	track zero
A26	IDE-CH1	5 i/o	IDE HD 3	B26	FLOPPY	5 i	write protected
A27	IDE-CH1	5 i/o	IDE HD 4	B27	FLOPPY	5 i	read data
A28	IDE-CH1	5 i/o	IDE HD 5	B28	FLOPPY	5 o	head select
A29	IDE-CH1	5 i/o	IDE HD 6	B29	FLOPPY	5 o	drive select 0
A30	IDE-CH1	5 i/o	IDE HD 7	B30	FLOPPY	5 o	motor on 0
A31	IDE-CH1	5 i/o	IDE HD 8	B31	APM	5 i	PWRBTN
A32	IDE-CH1	5 i/o	IDE HD 9	B32	IDE-CH1	5 o	IDE RESET#
A33	IDE-CH1	5 i/o	IDE HD 10	B33	APM	5 i	LID
A34	IDE-CH1	5 i/o	IDE HD 11	B34	USB	5 i/o	USB-P0+
A35	IDE-CH1	5 i/o	IDE HD 12	B35	USB	5 i/o	USB-P0-
A36	IDE-CH1	5 i/o	IDE HD 13	B36	IDE-CH1	5 o	A0
A37	IDE-CH1	5 i/o	IDE HD 14	B37	IDE-CH1	5 o	A1
A38	IDE-CH1	5 i/o	IDE HD 15	B38	IDE-CH1	5 o	A2
A39	IDE-CH1	5 o	IDE primary cs0#	B39	IDE-CH1	5 o	IORDY
A40	IDE-CH1	5 o	IDE primary cs1#	B40	LCD	5 o	LCD D32

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

= active low signal o.c. = open collector output NC = not connected

RES = pin function depending of the CPU, reserved

SM586PC Connector J2 Pin 41-80 (Vers. 2.1)

Pin	Group	Volt	Description	Pin	Group	Volt	Description
A41	PRINTER	5 o	PDACK#	B41	IrDA	5 o	IrDA TX (Fast)
A42	PRINTER	5 o	PREQ	B42	IrDA	5 i	IrDA RX (Fast)
A43	IDE-CH1	5 i	IRQ	B43	LCD	5 o	LCD D33
A44	IDE-CH1	5 o	IOR#	B44	LCD	5 o	LCD D34
A45	IDE-CH1	5 o	IOW#	B45	LCD	5 o	LCD D35
A46	POWER		VCC (5V)	B46	POWER	3 i	Battery 3.0V for RTC
A47	PCI	3 i/o	AD0	B47	PCI	3 i/o	AD16
A48	PCI	3 i/o	AD1	B48	PCI	3 i/o	AD17
A49	PCI	3 i/o	AD2	B49	PCI	3 i/o	AD18
A50	PCI	3 i/o	AD3	B50	PCI	3 i/o	AD19
A51	PCI	3 i/o	AD4	B51	PCI	3 i/o	AD 20 / IDSEL0
A52	PCI	3 i/o	AD5	B52	PCI	3 i/o	AD 21 / IDSEL1
A53	PCI	3 i/o	AD6	B53	PCI	3 i/o	AD 22 / IDSEL2
A54	PCI	3 i/o	AD7	B54	PCI	3 i/o	AD 23 / IDSEL3
A55	PCI	3 i/o	AD8	B55	PCI	3 i/o	AD 24
A56	PCI	3 i/o	AD9	B56	PCI	3 i/o	AD 25
A57	PCI	3 i/o	AD10	B57	PCI	3 i/o	AD 26
A58	PCI	3 i/o	AD11	B58	PCI	3 i/o	AD 27
A59	PCI	3 i/o	AD12	B59	PCI	3 i/o	AD 28 / IRQC
A60	PCI	3 i/o	AD13	B60	PCI	3 i/o	AD 29 / IRQA
A61	PCI	3 i/o	AD14	B61	PCI	3 i/o	AD 30 / IRQB
A62	PCI	3 i/o	AD15	B62	PCI	3 i/o	AD31
A63	PCI	3 o	C-BE0#	B63	PCI	3 i	PIRQA
A64	PCI	3 o	C-BE1#	B64	PCI	3 i	PIRQB
A65	PCI	3 o	C-BE2#	B65	PCI	3 i	PIRQC
A66	PCI	3 o	C-BE3#	B66	PCI	3 i	PIRQD
A67	POWER		VCC (5V)	B67	POWER		VCC (5V)
A68	PCI	3 o	PCI-CLK1	B68	PCI	3 o	PCI-CLK2
A69	PCI	3 i	REQ0#	B69	PCI	3 o	GNT0#
A70	PCI	3 i	REQ1#	B70	PCI	3 o	GNT1#
A71	PCI	3 i	REQ2#	B71	PCI	3 o	GNT2#
A72	PCI	3 i	REQ3#	B72	PCI	3 o	GNT3#
A73	RES		NC	B73	POWER		VCC (5V)
A74	PCI	3 i/o	FRAME#	B74	PCI	3 i/o	IRDY#
A75	PCI	3 i/o	TRDY#	B75	PCI	3 i/o	STOP#
A76	PCI	3 i/o	DEVSEL#	B76	PCI	3 i/o	PAR#
A77	PCI	3 i/o	SERR#	B77	PCI	3 i/o	LOCK#
A78	NC		NC	B78	PCI	3 o	PCI-RESET#
A79	CORE	3 i	resetinput / POWERgood	B79	ISA	5 i	DRQ7
A80	NC		NC	B80	ISA	5 0	DACK7

All PCI signals are left open, if the SmartModule does not support the PCI bus.

The SmartModule586PC does not support the PCI bus.

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

= active low signal o.c. = open collector output NC = not connected

RES = pin function depending of the CPU, reserved

SM586PC Connector J2 Pin 81-120 (Vers. 2.1)

Pin	Group	Volt	SM586PC	Pin	Group	Volt	SM586PC
A81	LCD	5 o	LCD D24	B81	USB	5 i/o	USB-P1+
A82	LCD	5 o	LCD D25	B82	USB	5 i/o	USB-P1-
A83	LCD	5 o	LCD D26	B83	USB	5 i/o	USB-OC0
A84	LCD	5 o	LCD D27	B84	USB	5 i/o	USB-OC1
A85	LCD	5 o	LCD D28	B85	ISA	5 o	LA22
A86	LCD	5 o	LCD D29	B86	ISA	5 o	LA23
A87	LCD	5 o	LCD D30	B87	PCI	5 i/o	PERR-
A88	LCD	5 o	LCD D31	B88	NC		NC
A89	NC		NC	B89	I2C	3 i/o	SMB-DAT
A90	NC		NC	B90	I2C	3 o	SMB-CLK
A91	POWER		3.3V	B91	POWER		3.3V
A92	NC		NC	B92	ISA	5 i	MASTER#
A93	NC		NC	B93	ISA	5 i	IOCHCK
A94	NC		NC	B94	IDE	5 i	CFlash DASP-
A95	NC		NC	B95	NC		NC
A96	APM	3 i	PWRBTN	B96	NC		NC
A97	NC		NC	B97	CORE	3 o	µP chip select PIIX4 (MCS-)
A98	APM	3 i/o	SUSA-	B98	APM	3 o	SUS-STAT1
A99	APM	3 i/o	SUSB-	B99	APM	3 o	SUS-STAT2
A100	APM	3 i/o	SUSC-	B100	APM	3 i	LID
A101	VGA	o	analog green	B101	VGA		analog ground
A102	VGA	o	analog blue	B102	VGA	o	vsynch
A103	VGA	o	analog red	B103	VGA	o	hsynch
A104	LCD	5 o	LCD ENAVEE	B104	LCD	5 o	LCD ENAVDD
A105	POWER		GROUND	B105	LCD	5 o	LCD SHCLK
A106	LCD	5 o	LCD FLM/VS	B106	LCD	5 o	LCD LP/HS
A107	LCD	5 o	LCD D12	B107	LCD	5 o	LCD D0
A108	LCD	5 o	LCD D13	B108	LCD	5 o	LCD D1
A109	LCD	5 o	LCD D14	B109	LCD	5 o	LCD D2
A110	LCD	5 o	LCD D15	B110	LCD	5 o	LCD D3
A111	LCD	5 o	LCD D16	B111	LCD	5 o	LCD D4
A112	LCD	5 o	LCD D17	B112	LCD	5 o	LCD D5
A113	LCD	5 o	LCD D18	B113	LCD	5 o	LCD D6
A114	LCD	5 o	LCD D19	B114	LCD	5 o	LCD D7
A115	LCD	5 o	LCD D20	B115	LCD	5 o	LCD D8
A116	LCD	5 o	LCD D21	B116	LCD	5 o	LCD D9
A117	LCD	5 o	LCD D22	B117	LCD	5 o	LCD D10
A118	LCD	5 o	LCD D23	B118	LCD	5 o	LCD D11
A119	LCD	5 o	LCD ENABKL	B119	LCD	5 o	LCD M
A120	POWER		LCD VCC (3V)	B120	POWER		CPU CORE (Vcc2)

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

= active low signal o.c. = open collector output NC = not connected

RES = pin function depending of the CPU, reserved

6.3 LCD Interface Signaldefinition

Pin 480BUS	LCD Line	Mono SS 8Bit	Mono DD 8Bit	Mono DD 16Bit	TFT 9/12/16Bit	TFT 18/24Bit	TFT HR 18/24Bit	STN DD 8Bit	STN DD 16Bit	TFT 36Bit
B107	D0	-	UD3	UD7	B0	B0	B00	R1	UR0	O-B0
B108	D1	-	UD2	UD6	B1	B1	B01	G1	UG0	O_B1
B109	D2	-	UD1	UD5	B2	B2	B02	B1	UB0	O-B2
B110	D3	-	UD0	UD4	B3	B3	B03	R2	UR1	O-B3
B111	D4	-	LD3	UD3	B4	B4	B10	G2	LR0	O-B4
B112	D5	-	LD2	UD2	G0	B5	B11	B2	LG0	O-B5
B113	D6	-	LD1	UD1	G1	B6	B12	R3	LB0	E-B0
B114	D7	-	LD0	UD0	G2	B7	B13	G3	LR1	E-B1
B115	D8	P0	-	LD7	G3	G0	G00	B3	UG1	E-B2
B116	D9	P1	-	LD6	G4	G1	G01	R4	UB1	E-B3
B117	D10	P2	-	LD5	G5	G2	G02	G4	UR2	E-B4
B118	D11	P3	-	LD4	R0	G3	G03	B4	UG2	E-B5
A107	D12	P4	-	LD3	R1	G4	G10	R5	LG1	O-G0
A108	D13	P5	-	LD2	R2	G5	G11	G5	LB1	O-G1
A109	D14	P6	-	LD1	R3	G6	G12	B5	LR2	O-G2
A110	D15	P7	-	LD0	R4	G7	G13	R6	LG2	O-G3
A111	D16	-	-	-	-	R0	R00	-	-	O-G4
A112	D17	-	-	-	-	R1	R01	-	-	O-G5
A113	D18	-	-	-	-	R2	R02	-	-	E-G0
A114	D19	-	-	-	-	R3	R03	-	-	E-G1
A115	D20	-	-	-	-	R4	R10	-	-	E-G2
A116	D21	-	-	-	-	R5	R11	-	-	E-G3
A117	D22	-	-	-	-	R6	R12	-	-	E-G4
A118	D23	-	-	-	-	R7	R13	-	-	E-G5
									-	
A81	D24									O-R0
A82	D25									O-R1
A83	D26									O-R2
A84	D27									O-R3
A85	D28									O-R4
A86	D29									O-R5
A87	D30									E-R0
A88	D31									E-R1
B40	D32									E-R2
B43	D33									E-R3
B44	D34									E-R4
B45	D35									E-R5
A106	VS/FLM	FRAME	S	FLM	VSYN	VSYN	VSYN	YD	YD	VS
B106	HS/LP	LOAD	CP1	CL1	HSYN	HSYN	HSYN	LP	LP	HS
B105	SHFCLK	CP	CP2	CL2	CK	CK	CK	XCKL	XCK	SH-Clk
B119	M	DF	-	M	ENAB	ENAB	-	-	-	M
PANEL		Generic	LM64P80 SHARP	LCM-5491 SANYO	LQ9D011 SHARP	LQ10D311 SHARP	LQ10DX01 SHARP	LM64C031 SHARP	LM64C08 Sharp	

6.4 CRT Monitor Signaldefinition

Pin:	Name:	Function:
A101	green	analog output green
A102	blue	analog output blue
A103	red	analog output red
B101	gnd	analog ground
B102	vsynch	vertical synchron signal to the CRT
B103	hsynch	horizontal synchron singla to the CRT

6.5 Connector Specifications

The DIGITAL LOGIC AG smartModule-586PC module connectors are surface mount 0.635mm pitch, 240pin connectors.

Parameter:	**Condition:**	**Specification:**
Material:	Contact: Housing:	Beryllium Copper Thermoplast Molded
Electrical:	Current:	0.5 Amp
	Voltage:	100 VAC
	Termination Resistance:	20mOhms
	Insulation Resistance:	500MOhm
Mechanical:	Mating Cycles:	50
	Connector Mating Force:	1N per contact
	Connector Unmating Force:	0.4N per contact
	Pitch:	0.635mm
	Number of pins:	240

The manufacturer of the connector is:

Source on SM586PC module *:	**Part-Name:**	**Part-Number:**
On customers board to hold a SM586PC h=5mm		
MOLEX 240pin		(53475-2409 *)
	Alternatives:	
	h=6mm (PCB-PCB)	(53467-2409 *)
	h=7mm (PCB-PCB)	(53481-2409 *)
SM586PC connector h=5mm		
MOLEX 240pin	Mating connector	52760-2409

* Only as a reference.

6.6 Thermal Specifications

Each product will undergo a BurnIn-Test of 10 cycles of 30 min. between the operating temperatures of –25°C to +70°C or higher if extended ranges are required.

The critical point is to meet the max. Tcase temperature of the CPU.

This temperature is specified by 110°C for the SQFP case. The tables show the allowable ambient temperature at various airflows and with different heatsink configurations.

CPU: 586 T (case) = 90°C Power consumption: 4W

CPU frequency	Air temperature	T case no Airflow 0 m/sec	T case Airflow 3 m/sec	T case Airflow 6 m/sec
166MHz	70°C			
266MHz	60°C			

These values have to be definitely defined when having series status !

7 DESIGNIN BLOCK SCHEMATICS

ATTENTION:

Very important information for smartModule integrators.

1. The minimum schematics to operate with the smartModule-586PC is described further on.
   Place on the 5Volt line 10x 100nF capacitors nearest possible at the powerpins.
2. Place on the 5Volt line 4 x 100uF/16V and 2 x 330µF tantal capacitors.
3. Use a separate ground and 5Volt plane in the OEM PCB.
4. If 3.3V DRAM extension are used, integrate a 3.3V powerplane to supply the DRAMs and other 3.3V parts.
   The 3.3V supply may be loaded with max. 300mA.
   Place also on the 3.3V plane 5 to 10 x 100nF and 2 x 100µF capacitors, nearest possible to the supply pins of each components.
   Place the DRAMs directly under the smartModule.
5. To meet all EMI/EMC parameters, place on every peripheral line (go to external cables) a ferrite (TDK) and a 47pF capacitor to ground.
6. All generic pullup resistor should be 10k typ
7. All generic buffers are recommended to be 74HCT245/244 or 74ABT245/244 type.
8. If using SODIMM's, please refer to our overview list, which is also on our CD. Cleaning the contacts on the SODIMM and the socket with e.g. pure alcohol is highly recommended to may eliminate memory errors.
9. For any questions, we are providing a DesignIn support. Please fill out the form in chapter 1.6 to initialize a DesignIn support

On the next pages, one will find designIn recommendations taken from various INTEL manuals.

7.1 INTEL 430TX

7.1.1 Architecture overview

The MTXC host bridge provides a completely solution for the system controller and datapath components in a Pentium processor system. The MTXC Supports all Pentium family processors since P54C, it has 64-bit Host and DRAM Bus Interface, 32-bit PCI Bus Interface, Second level Chache Interface, and it integrates the PCI arbiter.

The MTXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus (see Figure 1).

The MTXC bus interfaces are designed to interface with 2.5V, 3.3V and 5V busses. The MTXC implements 2.5V and 3.3V drivers and 5V tolerant receivers. The MTXC connects directly to the Pentium processor 3.3V or 2.5V host bus, directly to 5V or 3.3V DRAMs, and directly to the 5V or 3.3V PCI bus. The 430TX also interfaces directly to the 3.3V or 5.0V TAGRAM and 3.3V Cache.

The MTXC works with the PCI IDE/ISA Accelerator 4 (PIIX4). The PIIX4 provides the PCI-to-ISA/EIO bridge functions along with other features such as a fast IDE interface (PIO mode 4 and Ultra DMA/33), Plug-n-Play port, APIC interface, PCI 2.1 Compliance, SMBUS interface, and Universal Serial Bus Host Controller functions.

7.1.2 DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard (or Fast) Page Mode (FPM), Extended Data Out (EDO) and Synchronous DRAM (SDRAM) memory. The DRAM controller inside the MTXC is capable of generating 3-1-1-1 for posted writes for any type of DRAM that is used. While read performance is 6-1-1-1 for SDRAM, 5-2-2-2 for EDO, and 6-3-3-3 for FPM.

The DRAM interface supports 4 Mbytes to 256 Mbytes with six RAS lines. The MTXC supports 4-Mbit, 16-Mbit, and 64-Mbit DRAM and SDRAM technology, both symmetrical and asymmetrical. Parity is not supported, and for loading reasons, x32 and x64 SIMMs/DIMMs/SO-DIMMs should be used.

7.1.3 Second Level Cache

The second level cache is direct mapped and supports both 256-Kbyte and 512-Kbyte SRAM configuration using Pipeline Burst SRAM or DRAM Cache SRAM. The Cache performance is 3-1-1-1 for line read/write and 3-1-1-1-1-1-1-1 for back to back reads that are pipelined. Cacheless configuration is also supported.

7.1.4 PCI Interface

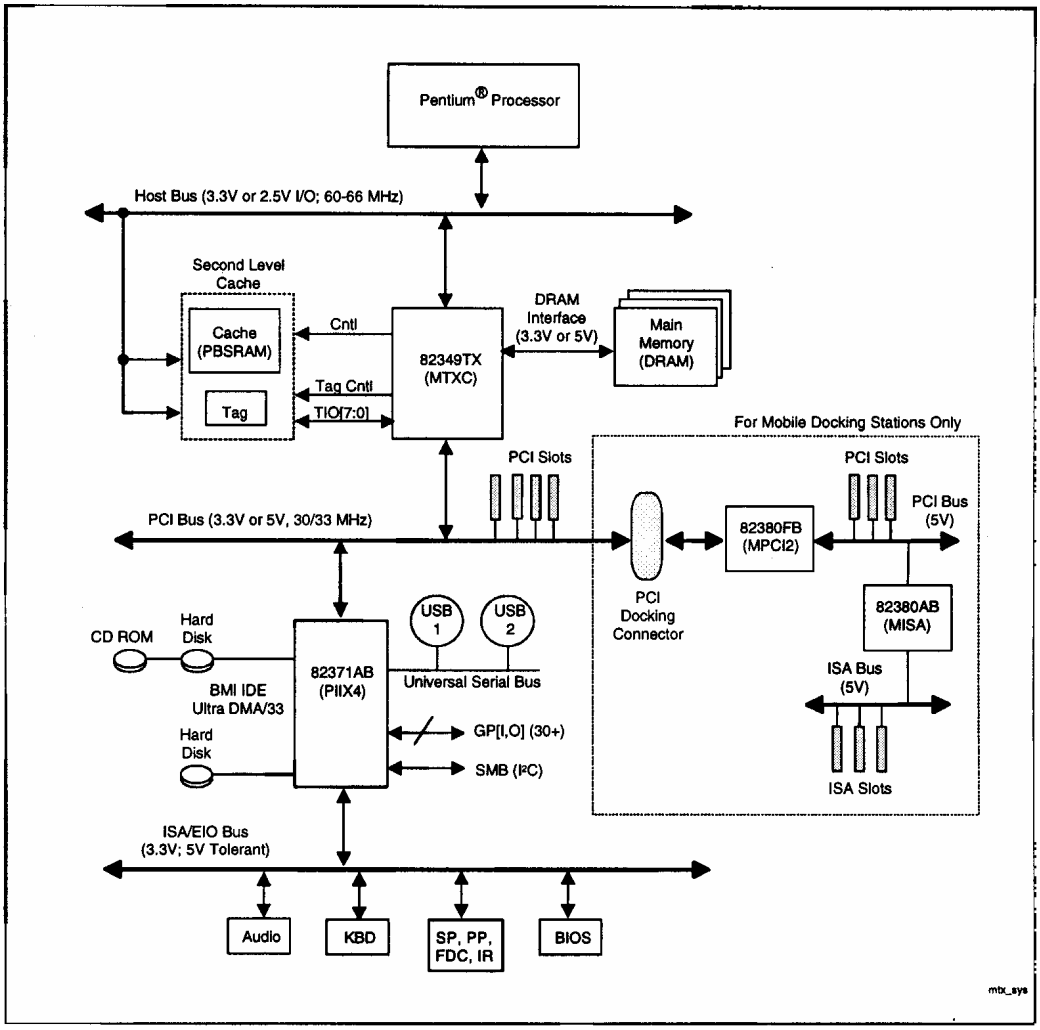
The PCI interface is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX4 bus master requests.

7.1.5 Datapath and Buffers

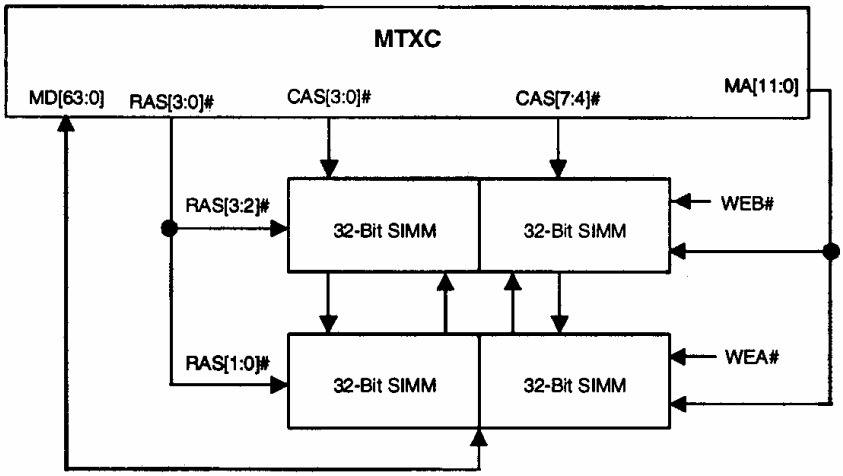
The MTXC contains three sets of data buffers for optimizing data flow. A five QWord deep DRAM write buffer is provided for CPU-to-DRAM writes, second level cache write backs, and PCI-to-DRAM transfers. This buffer is used to achieve 3-1-1-1 posted writes to DRAM and also provides DWord merging and burst merging for CPU-to-DRAM write cycles. In addition, an extra line of buffering is provided that is combined with the DRAM Write Buffer to supply an 18 DWord deep buffer for PCI to main memory writes. A five DWord buffer is provided for CPU-to-PCI writes to help maximize the bandwidth for graphic writes to the PCI bus. Also, five QWords of prefetch buffering has been added to the PCI-to-DRAM read path that allows up to two lines of data to be prefetched at an x-2-2-2 rate. The MTXC interfaces directly to the Host and DRAM data bus.

7.1.6 Power Management Features

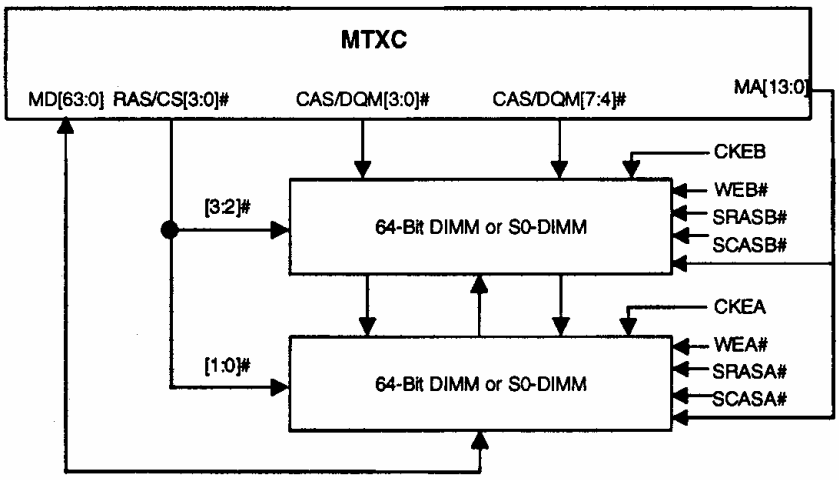
The MTXC implements extensive power management features. The CLKRUN# feature enables controlling of the PCI clock (on/off). The MTXC supports POS, STR, STD, and Soft-off suspend states. SUSCLK and SUSSTAT1# signals are used for implementing Suspend Logic. The MTXC supports two SMRAM modes; Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). The C_SMRAM is the traditional SMRAM feature implemented in Intel PCIsets. The E_SMRAM is a new feature that supports writeback cacheable SMRAM Space up to 1 Mbytes. In order to minimize the idle power, the internal clock in MTXC is turned off (gated off) when there is no activity on the Host and PCI Bus.



7.1.7 430TX FPM/EDO Four Row SIMM Configuration



7.1.8 430TX EDO/SDRAM four row DIMM or SO-DIMM Configuration



NOTES:

1. In a configuration that supports suspend to RAM, only CKE is used. This is because CKEB is not part of the suspend well the MTXC maintains during a suspend to RAM state.
2. In a desktop system that supports EDO/FPM, CKE and CKEB should be used as the second pair of MA0 and MA1 lines. CKE is used as MAA0 and CKEB is used as MAA1. In this case, they should be evenly distributed throughout the system along with the first pair of MA0 and MA1 lines.

7.2 PCI-Bus

7.2.1 PCI Bus Signals

The smartModule supports 3.3 and 5V PCI.

An 8.2 KΩ - 10 KΩ pull-up to V_3S should be placed on the CLKRUN# signal.

7.2.2 Design Considerations

The smartModule supports up to four PCI masters with its REQ[3:0]#/GNT[3:0]# pairs (the 82443TX GNT4/REQ4 is not supported). The PCI bus supports up to 10 PCI loads. The 82443TX/TX and the PIIX4E each represent one load; other PCI components soldered on the motherboard add one load each; and each PCI connector adds approximately 2 loads. A design with four PCI slots and no motherboard devices uses all available PCI loads. When all four REQ[3:0]#/GNT[3:0]# pairs are used, simulation is required to ensure that the PCI Bus Specification Rev. 2.1 timings are met. It is recommended, per PCI specification, that the design have series resistors (~100Ω) on each of the PCI connector IDSEL lines.

PCI Bus Signals Resistor Values

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω) external used
AD[31:0]	None	None
C/BE[3:0]	None	None
FRAME#	None	10 K pull-up to V_3S
DEVSEL#	None	10 K pull-up to V_3S
IRDY#	None	10 K pull-up to V_3S
TRDY#	None	10 K pull-up to V_3S
STOP#	None	10 K pull-up to V_3S
REQ[4:0]#	None	10 K pull-up to V_3S if unused
GNT[4:0]#	None	10 K pull-up to V_3S if used
PHOLD#	None	10 K pull-up to V_3S
PHLDA#	None	10 K pull-up to V_3S
PAR	None	None
SERR#	None	10 K pull-up to V_3S
CLKRUN#	None	8.2 ~ 10 K pull-up to V_3S
PCIRST#	33 (see „PCI Bus Signals“)	None
PLOCK#	None	10 K pull-up to V_3S

7.2.3 PCI Signal Descripitons

Name	Type	Voltage	Description
AD[31:0]	I/O PCI	V_3	Address/Data: The standard PCI address and data lines. The address is driven with FRAME# assertion, and data is driven or received in following clocks.
C/BE[3:0]#	I/O PCI	V_3	Command/Byte Enable: The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the following clocks.
FRAME#	I/O PCI	V_3	Frame: Asseriton indicates the address phase of a PCI transfer. Negation indicates that one more data transfers are desired by the cycle initiator.
DEVSEL#	I/O PCI	V_3	Device Select: This signal is driven by the 443TX Host Bridge when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O PCI	V_3	Initiator Ready: Asserted when the initiator is ready for data transfer.
TRDY#	I/O PCI	V_3	Target Ready: Asserted when the target is ready for a data transfer.
Stop#	I/O PCI	V_3	Stop: Asserted by the target to request the master to stop the current transaction.

PCI Signal Descriptions (continued)

Name	Type	Voltage	Description
PLOCK#	I/O PCI	V_3	Lock: Indicates an exclusive bus operation and may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed. The 443TX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
REQ[4:0]#	I PCI	V_3	PCI Hold: PCI master requests for PCI.
GNT[4:0]#	O PCI	V_3	PCI Grant: Permission is given to the master to use PCI.
PHOLD#	I PCI	V_3	PCI Hold: This signal comes from the expansion bridge; it is the bridge request for PCI. The 443TX Host Bridge will drain the DRAM write buffers, drain the processor-to-PCI posting buffers, and acquire the host bus before granting the request via PHLDA#. This ensures that GAT timing is met for ISA masters. The PHOLD# protocol has been modified to include support for passive release.
PHLDA#	O PCI	V_3	PCI Hold Acknowledge: This signal is driven by the 443TX Host Bridge to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release.
PAR#	I/O PCI	V_3	Parity: A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	I/O PCI	V_3	System Error: The 443TX asserts this signal to indicate an error condition. Please refer to the Intel 430TX AGPset datasheet (Order Number 290633-001) for further information.
CLKRUN#	I/O D PCI	V_3	Clock Run: An open-drain output and also an input. The 443TX Host Bridge requests the central resource (PIIX4E) to start or maintain the PCI clock by asserting CLKRUN#. The 443TX Host Bridge tri-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset).
PCI_RST#	I CMOS	V_3	Reset: When asserted, this signal asynchronously resets the 443TX Host Bridge. The PCI signals also tri-state, compliant with PCI Rev 2.1 specifications.

7.3 PIIX4 and Sideband-Bus

Processor/PIIX4E ISA Bridge Sideband Signals

Pull-ups to V_CPUPU: INIT# - 1 KΩ, STPCLK# - 680Ω; LINT1#/NMI, LINT0#/INTR# IGNNE#, A20M#, SMI# - 4.7KΩ. These are open collector outputs from the PIIX4A component.

CPURST can be left unconnected for smartCoreP3 designs.
CPURST must be connected to the PIIX4 for smartCore586 designs.

Refer to the *System Management Bus Specification* for descriptions and specifications of the three SMBus signals: SMBALERT#, SMBCLK, and SMBDATA. A pull-up resistor is required. Values will vary depending on V_{DD} and the actual capacitance of the bus.

7.3.1 Sideband Signal Resistor Value

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω) in the smartModule
FERR#	None	None
CPURST	None	None
IGNNE#	None	4.7 K pull-up to V_CPUPU
INIT#	None	1 K pull-up to V_CPUPU
INTR	None	4.7 K pull-up to V_CPUPU
NMI	None	4.7 K pull-up to V_CPUPU
A20M#	None	4.7 K pull-up to V_CPUPU
SMI#	None	4.7 K pull-up to V_CPUPU
STPCLK#	None	680 pull-up to V_CPUPU

7.3.2 Sideband Signals

Name	Type	Voltage	Description
FERR#	O CMOS	V_CPUPU	Numeric Coprocessor Error: This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the processor and is driven by the processor to the PIIX4E.
IGNNE#	I D CMOS	V_CPUPU	Ignore Error: This open drain signal is connected to the ignore error pin on the processor and is driven by the PIIX4E.
INIT#	I D CMOS	V_CPUPU	Initialization: INIT# is asserted by the PIIX4E to the processor for system initialization. This signal is an open drain.
INTR	I D CMOS	V_CPUPU	Processor Interrupt: INTR is driven by the PIIX4E to signal the processor that an interrupt request is pending and needs to be serviced. This signal is an open drain.
NMI	I D CMOS	V_CPUPU	Non-Maskable Interrupt: NMI is used to force a non-maskable interrupt to the processor. The PIIX4E ISA bridge generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. This signal is an open drain.
A20M#	I D CMOS	V_CPUPU	Address Bit 20 Mask: When enabled, this open drain signal causes the processor to emulate the address wraparound at one Mbyte which occurs on the Intel 8086 processor.
SMI#	I D CMOS	V_CPUPU	System Management Interrupt: SMI# is an active low synchronous output from the PIIX4E that is asserted in response to one of many enabled hardware or software events. The SMI# open drain signal can be an asynchronous input to the processor. However, in this chip set SMI# is synchronous to PCLK.
STPCLK#	I D CMOS	V_CPUPU	Stop Clock: STPCLK# is an active low synchronous open drain output from the PIIX4E that is asserted in response to one of many hardware or software events. STPCLK# connects directly to the processor and is synchronous to PCICLK. When the processor samples STPCLK# asserted it responds by entering a low power state (Quick Start). The processor will only exit this mode when this signal is deasserted.

7.4 Powermanagement

7.4.1 Power Management Signals Resistor Values

Name	Termination Resistor (Ω)	Pull-up (Pull-down) Resistor (Ω)
SUS_Stat#	None	None
SHDN	None	None
PWRGOOD	None	None
SM_CLK	None	Refer to the *System Management Bus Specification*
SM_DATA	None	Refer to the *System Management Bus Specification*

7.4.2 Power Management Signals

Name	Type	Voltage	Description
SUS-STAT1#	I CMOS	V_3ALWAYS*	Suspend Status: This signal connects to the SUS_STAT1# output of PIIX4E. It provides information on host clock status and is asserted during all suspend states.
PWRGOOD	O	V_3S	PWRGOOD: This signal is driven high by the Intel Mobile Module to indicate the voltage regulator is stable and is pulled low using a 131.6K resistor when inactive. It can be used in some combination to generate the system PWRGOOD signal.
SM_CLK	I/O D CMOS	V_3	Serial Clock: This clock signal is used on the SMBUS interface to the digital thermal sensor.
SM_DATA	I/O D CMOS	V_3	Serial Data: Open-drain data signal on the SMBUS interface to the digital thermal sensor.
LM75_INT#	O D CMOS	V_3	ATF Interrupt: This signal is an open-drain output signal of the digital thermal sensor.

7.5 Clocks

7.5.1 Clock Layout Guidelines

Series matching resistors are required.
Resistor Value: See Table 7.
Placement: As near as possible to the driver pin (less than 1“).

- A PCLK that is used for a PCI socket should be a point-to-point connection and should not be shared with another load.
- When designing with an expansion connector, remember to account for the PCICLK trace length in the docking station.
- Route all clocks on internal layers to provide better trace delay consistency and EMI containment.
- Board impedance should be 55 Ω ± 15%.
- Use discrete resistors on HCLK signals coming from CK100-M.
- Minimize the use of vias in clock signals.
- All clocks should have 1:2 width-to-spacing ratio.
- CKBF-M should be on the V_3 rail and CK100-M should be on the V_3S rail (see „Power and Ground Pins“ on page 34 for a description of these rails).

7.5.2 Clock Signals

Name	Type	Voltage	Description
PCLK	I PCI	V_3S	PCI Clock In: PCLK is an input to the module is one of the system’s PCI clocks. This clock is used by all of the 443TX Host Bridge logic in the PCI clock domain. This clock is stopped when the PIIX4E PCI_STP# signal is asserted and/or during all suspend states.
DCLKO	O CMOS	V_3	SDRAM Clock Out: 66 MHz SDRAM clock reference generated internally by the 443TX Host Bridge system controller onboard PLL. It feeds and external buffer that produces multiple copies for the SO-DIMMs.
DCLKI	I CMOS	V_3	SDRAM Read Clock: Feedback reference from the SDRAM clock buffer. This clock is used by 443TX Host Bridge System Controller when reading data from the SDRAM array.

7.6 ITP / JTAG Signals

Name	Type	Voltage	Description
TDO	O	V_CPUPU	JTAG Test Data Out: Serial output port TAP instructions and data are shifted out of the processor from this port
TDI	I	V_CPUPU	JTAG Test Data In: Serial input port. TAP instructions and data are shifted into the processor from this port.
TMS	I	V_CPUPU	JTAG Test Mode Select: Controls the TAP controller change sequence.
TCLK	I	V_CPUPU	JTAG Test Clock: Testability clock for clocking the JTAG boundary scan sequence.
TRST#	I	V_CPUPU	JTAG Test Reset: Asynchronously resets the TAP controller in the processor.
VCCT	O	V_Core	GTL+ Termination Voltage: Used by the POWERON pin on the ITP debug port to determine when target system is on. POWERON pin is pulled up using a 1KΩ resistor to VTT.

7.7 Clock and Test Signals

USB Clock – A 48 MHz clock with a duty cycle of better than 40/60% should be fed into the PIIX4E's USB clock input, pin L3.

Place a 10- KΩ pull-up resistor on TEST# to V_3ALWAYS. Test signals reside in the Suspend/Resume well.

In a Pentium II processor-based system, CONFIG[1] should be pulled to V_3ALWAYS with a 100- KΩ resistor.

CONFIG[2] should be pulled to GND with a 100- KΩ resistor in all 430TX AGPset-based designs.

Clock and Test Signal Resistor Values

Name	Termination Resistor (Ω)	Pull-up (pull-down) Resistor (Ω)
TEST#	None	10 K Pull-up to V_3ALWAYS
CONFIG[1]	None	100 K Pull-up to V_3ALWAYS
CONFIG[2]	None	10 K Pull-down

7.8 PCI Bus Signals

- All unused general purpose inputs (GPIs) should be pulled to a valid logic level with a 10- KΩ resistor. When pulled high, they should be pulled to V_3S expect for the GPIs that are in the V_{CC} (SUS) well.
- All unused outputs can be left as no-connects.
- All IDSEL signals should have a 100-W series resistor at each device.
- In a 5-V PCI environment, place 2.7 KΩ pull-up resistors to 5-V on PIRQ[A:D]#, SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, REQ64# and ACK64# on the PCI bus.
- Place the 10-KΩ pull-up resistors to V_3S on PCIREQ[D:A]# and REQ[A:C]# when these signals are unused or when using a PCI add-in slot to insure that these signals do not float.
- In a 3.3-V PCI environment , place 10-KΩ pull-up resistors to V_3S on PIRQ[A:D]# , SDONE, SBO#, FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, PERR#, SERR#, REQ64# and ACK64# on the PCI bus.
- For all new designs, make sure that the PIIX4E does not connect IDSEL to AD12, becoming device 1. On 82443TX, AGP is known as device 1 whether disabled or not. Connect IDSEL from PIIX4E to AD18.
- For systems in which the PCIRST# signal is lightly loaded (<50pF), place a 33-W series termination resistor on this signal. This resistor should be placed as close as possible to the PIIX4E.

PCI Bus Signal Resistor Values, (onboard smartModule)

Name	Termination Resistor (Ω)	Pull-up (pull-down) Resistor (Ω)
Unused GPIs	None	10 K to a valid level
IDSEL signals	100	None
PIRQ[A:D]#	None	10 K Pull-up to V_3S
SDONE	None	10 K Pull-up to V_3S
SBO#	None	10 K Pull-up to V_3S
FRAME#	None	10 K Pull-up to V_3S
TRDY#	None	10 K Pull-up to V_3S
STOP#	None	10 K Pull-up to V_3S
IRDY#	None	10 K Pull-up to V_3S
DEVSEL#	None	10 K Pull-up to V_3S
PLOCK#	None	10 K Pull-up to V_3S
PERR#	None	10 K Pull-up to V_3S
SERR#	None	10 K Pull-up to V_3S
REQ64#	None	10 K Pull-up to V_3S
ACK64#	None	10 K Pull-up to V_3S
PCIREQ[D:A]#	None	10 K Pull-up to V_3S
REQ[A:C]#	None	10 K Pull-up to V_3S

7.9 ISA/EIO Signals

- When implementing Power On Suspend (POS) mode, ISA signals should be pulled up to V_3S. Otherwise use V_5S.
- Use 10 KΩ pull-up resistors on SD[15:0], MEMR#, MEMW#, IOR#, IOW#, IOCS16#.
- Use 1 KΩ pull-up resistors on IOCHRDY, MEMCS16#, REFRESH#, ZEROWS#.
- Use 10 KΩ pull-up resistors on IRQx. IRQ8# resides in the V_{CC} (SUS) well, it must be pulled to V_3ALWAYS. When IRQ8# is not used, its default is GPI[6] and it requires a 10 KΩ external pull-up resistor.
- Use a 4.7 KΩ pull-down resistor on DRQx.
- When using the EIO bus, IOCHK# becomes a general-purpose input and in ISA, IOCHK# requires a 4.7 KΩ pull-up resistor.

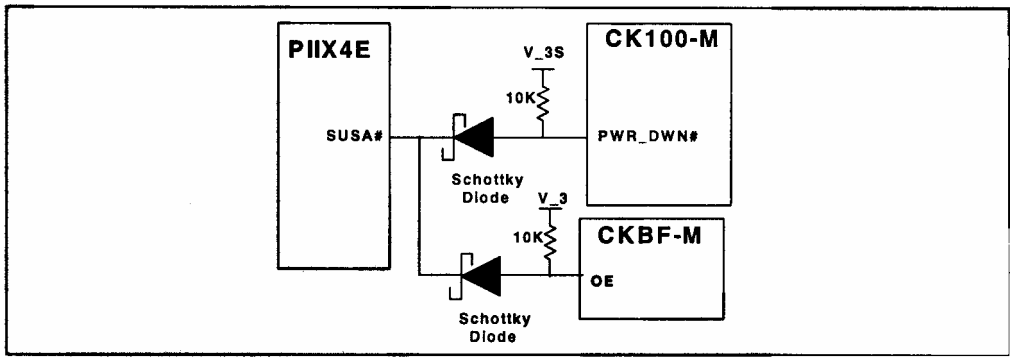
ISA/EIO Signal Resistors Values

Name	Termination Resistor (Ω)	Pull-up (pull-down) Resistor (Ω)
SAD15:0]	None	10 K Pull-up to V_3S
MEMR#	None	1 K Pull-up to V_3S
MEMW#	None	1 K Pull-up to V_3S
IOR#	None	1 K Pull-up to V_3S
IOW#	None	1 K Pull-up to V_3S
IOCS16#	None	1 K Pull-up to V_3S
IOCHRDY	None	1 K Pull-up to V_3S
MEMCS16#	None	1 K Pull-up to V_3S
REFRESH#	None	1 K Pull-up to V_3S
ZEROWS#	None	1 K Pull-up to V_3S
IRQx	None	10 K Pull-up to V_3S (see above)
DRQx	None	4.7 K (Pull-down)
SIRQ	None	10 K Pull-up to V_3S
IOCHK#	None	4.7 K Pull-up (if using ISA bus)

7.10 Power Management Signals

- Power management signals that reside in the V_{CC} (SUS) well may require pull-ups, the pull-ups must be connected to V_3ALWAYS. These signals do not support 5-V input levels.
- EXTSMI# is an input at reset and open drain output when activating an SMI# within the serial IRQ function. Designs may need an 8.2 KΩ pull-up to V_3ALWAYS when it is not always being driven to a valid state.
- When CLKRUN# is not connected between the PIIX4E and the 82443TX, it should be tied low through a 100 Ω resistor at the 82443TX. When CLKRUN# is connected between the PIIX4E and the 82443TX, an 8.2 KΩ - 10 KΩ pull-up to V_3S should be placed on the CLKRUN# signal.
- SUS_STAT1# is connected between the 82443TX and PIIX4E.
- PCI_STP# is connected to the clock synthesizer to stop the PCI clocks.
- CPU_STP# is connected to the clock synthesizer to stop the processor clock.
- SUSA# is connected to the clock synthesizer's PWR_DWN# pin through a Schottky diode with a 10 KΩ pull-up resistor. Alternatively, SUSA# may be used to control the clock synthesizer's power plane.

Clock Design Block Diagram



- SUSB# and SUSC# are used to control the power planes.
- THRM# is connected to the thermal protection logic.
- PCIREQ[D:A]# is connected between the PIIX4E and the PCI bus. Bus master requests are considered to be power management events.
- Connect RI# to the modem when this feature is used.
- Connect BATLOW# to the battery monitoring logic when this feature is implemented.
- Connect LID to the lid monitoring logic of the system.
- PWRBTN# is connected to logic that allows the user to switch from and to suspend.
- RSMRST# is connected to a switch to allow a complete system reset. This signal resides in the V_{CC} (RTC) well. Its potential must not exceed that of V_{CC} (RTC).

Power Management Signal Resistor Values

Name	Damping Resistor (Ω)	Pull-up (pull-down) Resistor (Ω)
EXTSMI#	None	See above
CLKRUN#	None	8.2 KΩ ~ 10 KΩ Pull-up to V_3S (if connected from PIIX4E to 82443TX) 100 KΩ (Pull-down) otherwise

7.11 USB Interface

Refer to the *PIIX4 USB Design Guide* for the layout recommendations for USB, clock, over-current detection circuit and general board layout recommendations.

7.12 IDE Interface

- 5.6 KΩ pull-down resistors on PDDREQ and SDDREQ.
- 1 KΩ pull-up resistors on PIORDY and SIORDY.
- 470 KΩ pull-down resistors on pin 28 of the IDE connector (CSEL). Support Cable Select (CSEL) is a PC97 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
- The primary IDE connector uses IRQ14, and the secondary IDE connector uses IRQ15.
- The ATA-4 specification requires 33 Ω series terminating resistors on P/SDIOR, P/SDIOW#, P/SDCS[1,3]#, P/SDA[2:0], P/SDDACK# and P/SDD[15:0]. These series termination resistors should be placed as close as possible to the PIIX4E.
- For Ultra-DMA enabled systems, the ATA-4 specification also requires 82 Ω series termination resistors on P/SDDREQ, INTRQx and P/SIORDY. These series terminating resistors should be placed as close as possible to the PIIX4E.
- When the distance between the PIIX4E and connector is greater than 4”, the terminating resistors should be placed within 1” of the PIIX4E.
- When using the ISA reset signal RSTDRV from the PIIX4E, it should be routed through a Schmitt trigger for RESET# signals.
- Ground pins 19, 2, 22, 24, 26, 30, 40 of both ATA connectors.
- Pins 20 and 34 of both ATA connectors should be left unconnected.
- According to ATA-4 specification, a 10 KΩ pull-down resistor is required on DD7 to allow a host to recognize the absence of a device at power-up.
- Exceptions: When the PIIX4E’s IDE interface is configured as Primary 0/Primary 1, and two IDE devices are connected, it should appear to the devices as if they are on the same cable. See *intel ® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4)* datasheet (order number 290562).
- Both IDE devices should connect to IRQ14.
- CSEL connected (pin 28) together between the two ATA connectors and be pulled down with a 470 Ω resistor to meet PC97 requirement.
- DIAG (pin 34) connected together between the two ATA connectors.

•

IDE Interface Signal Resistor Values

Name	Termination Resistor (Ω)	Pull-up (pull-down) Resistor (Ω)
PDDREQ	33 (82 for Ultra DMA)	5.6 K (pull-down)
SDDREQ	33 (82 for Ultra DMA)	5.6 K (pull-down)
PIORDY	82 (Ultra DMA only)	1 K Pull-up
SIORDY	82 (Ultra DMA only)	1 K Pull-up
CSEL (Pin 28)	None	470 (pull-down)
All signals to the two IDE connectors	33	None
DD7	33	10 K (pull-down)

7.13 BIOS to Flash Memory Interface

- 2 Mbits of flash is usually all that is required to support the 82443TX in all configurations. These are the recommendations for an Intel 28F200BV flash part.

- Use 0.01 µF – 0.1 µF capacitors for power supply (V_{CC} and V_{pp}) decoupling.
- Connect BYTE# to GND when a x16 flash device is used to confîgure it for x8.
- Use GPO*x* to control the WP# signal.
- Connect V_{pp} to 5-V.
- Use GPO*x* to control the RP# signal.

Power Sequencing

This section provides a summary of the power sequencing requirements and options of the 430TX AGPset. It provides a detailed description of the PIIX4E Suspend/Resume sequence, signaling protocols, and timings. The recommended usage model for power plane control in a 430TX platform using PIIX4E power management signals is described.

This section does not represent the only way to design a system, but it does provide recommendations for using the 430TX AGPset.

7.13.1 Suspend/Resume and Power Plane Control

The PIIX4E supports three different Suspend modes. The common system usage model for these modes is described here and includes Power On Suspend (POS), Suspend to RAM (STR), and Suspend to Disk (STD). This mode definition allows for other system usage models that use the PIIX4E suspend/resume control signals in other ways. The common system mode names are used throughout this document.

The PIIX4E power management architecture is designed to allow systems to support multiple suspend modes, and to switch between those modes as required. A suspended system can be resumed by a number of different events. The system returns to full operation, and can then continue processing or be placed into another suspend mode. The new mode can be at a lower power mode than from what it resumed.

7.13.2 Power On Suspend (POS) System Model

All devices are powered up except for the clock synthesizer. The Host and PCI clocks are inactive, and the PIIX4E provides control signals and the 32 KHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer. The only power consumed in the system while it is in POS mode is due to DRAM refresh and leakage current of the powered devices.

When the system resumes from POS mode, the PIIX4E can resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, the PIIX4E only needs to wait for the clock synthesizer and processor PLLs to lock before the system is.

7.13.3 Suspend to RAM (STR)

Power is removed from most of the system components during STD. Power is maintained to the RTC and Suspend Well logic in the PIIX4E.

The PIIX4E resets the system on resume from STD.

The STD state is also called the Soft Off (SOff) state. The difference depends on whether the system state is restored by software to a pre-suspend condition or if the system is rebooted.

7.13.4 Mechinical Off (MOff)

This is not a suspend state. This is a condition where all power except the RTC battery has been removed from the system. It is typically controlled by a mechanical switch that turns off AC power to a power supply. It could be used as a condition in which an embedded system's main battery has been removed.

The PIIX4E controls the system entering the various suspend states through the suspend control signals listed in Table 26. Upon initiation of suspend, the PIIX4E asserts the SUS_STAT[1-2]#, SUSA#, SUSB#, and SUSC# signals in a well defined sequence to switch the system into the desired power state. The SUSA#, SUSB#, and SUSC# signals can be used to control various power planes in the system. The SUS_STAT1# signal is a status signal that indicates to the host bridge when to enter or exit a suspend state, or when to enter or exit a stop clock state (when the system is still running). This is typically used to place the DRAM controller into a Suspend Refresh mode of operation. The SUS_STAT2# signal is a status signal that can be used to indicate to other system devices when to enter or exit a suspend state (like the graphics and Card-bus controllers). See

"System Suspend and Resume Control Signaling" on page 50 for sequencing details. Note that these signals are associated with a particular type of suspend mode and power plane for descriptive purposes here. The system designer is free to use these signals to control any type of function desired

The system is placed into a suspend mode by programming the Power Management Control register. The Suspend Type is first programmed and then the Suspend Enable bit is set. This causes the PIIX4E to automatically sequence into the programmed suspend mode.

Power State Decode

Power State	RSMRST#	SUS_STAT1#	SUS_STAT2#	SUSA#	SUSB#	SUSC#
On	1	X†	1	1	1	1
POS	1	0	0	0	1	1
STR	1	0	0	0	0	1
STD/SOFF	1	0	0	0	0	0
Mechanical Off	0	0	0	0	0	0

SUS_STAT1# is also used when the system is running. It indicates to the Host-to-PCI bridge when to switch between the normal and suspend refresh mode for DRAM Stop Clock support. In the Stop Clock condition, HCLK is stopped and the Host-to-PCI bridge must run DRAM refresh from the internal oscillator.

7.13.5 System Resume

The PIIX4E can be resumed from either a Suspend or Soft Off state. Depending on the suspend state that the system is in, different features can be enabled to resume the system . There are two classes of resume events, those whose logic resides in the PIIX4E main power well and those whose logic resides in the PIIX4E suspend well. Those in the suspend well can resume the system from any Suspend or Soft Off state. Those in the main power well can only resume the system from a Power On Suspend state. Table 27 lists the suspend states for which a particular resume event can be enabled.

Upon detection of an enabled resume event, the PIIX4E sets appropriate status signals and automatically transitions its suspend control signals to bring the system into a “full on” condition. The sequencing is shown in “System Suspend and Resume Control Signaling” on page 50.

Resume Events Supported In Different Power States

	Suspend States			
Resume Events	POS	STR	STD/SOff	MOff
RTC Alarm (IRQ8)†	X	X	X	
SMBus Resume Event (Slave Port Match)	X	X	X	
Serial A Ring (RI)	X	X	X	
Power Button (PWRBTN#)	X	X	X	
EXTSMI (EXTSMi#)	X	X	X	
LID (LID)	X	X	X	
GPI 1	X	X	X	
GSTBY Timer Expiration	x	X	X	

Resume Events Supported In Different Power States

	Suspend States			
Resume Events	POS	STR	STD/SOff	MOff
Interrupt (IRQ 1, 3-15)	X			
USB	X			

RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GP[1], LID, EXTSMI#, RI#) for the resume functionality.

Systeme Resume Events

The various resume events and their programming model are shown here.

Resume Event Programming Model

System Resume Event	Programming Model
PWRBTN# Asserted	[PWRBTN_EN]
LID Asserted - Polarity Select	[LID_EN] [LID_POL]
GP[1] Asserted	[GPI_EN]
EXTSMI# Asserted	[EXTSMI_EN]
SMBus Events:	[ALERT_EN] [SLV_EN] [SHDW1_EN] [SHDW2_EN]
Global Standby Timer Expiration:	[GSTBY_EN]
Ring Indicate Assertion (RI#)	[RI_EN]
RTC Alarm (IRQ8)†	[RTC_EN]
USB Resume Signaling: (POS Only)	[USB_EN]
IRQ [1,3-7, 9-15]: (POS Only)	[IRQ_RSM_EN!

RTC Alarm only supports internal RTC. For external RTC implementations, the IRQ8 must be tied to one of the other resume input signals (GPI[1], LID, EXTSMI#, RI#) for the resume functionality.

Global Standby Timer Resume

The Global Standby Timer is used to monitor system activity during normal operation and can be reloaded by system activity events. Upon expiration, it generates an SMI#. When the system is placed in a Suspend Mode, the Global Standby Timer can be used to generate a resume event. The Global Standby Timer can enable two different timer resolutions for wake-up times from approximately 30 seconds to 8.5 hours. This can allow the system to transition into a lower power suspend state.

See the System Management Section of the *82371AB PCI-to-ISA/DIE Xcelerator* (PIIX4) datasheet for additional information about the Global Standby Timer.

7.13.6 System Suspend and Resume Control Signaling

The PIIX4E automatically controls the signals required to transition the system between the various power states. It provides control for Host and PCI clocks, main memory and video memory refresh, system power plane control, and system reset. Table 29 and Table 30 illustrate the common usage model for power plane control using the SUS[C:A]# signals. The PIIX4E Resume well should always be powered by a trickle supply (main battery or backup battery in an embedded system).

Power Plane Control

SUSA# (POS)	SUSB# (STR)	SUSC# (STD)
Clock synthesizer Video display [1]	Processor (Low Power GTL+supplies) PIIX4E Core Other system devices [2]	82443TX Host Bridge Controller DRAM Graphics Controller

Notes:
The video display (flat panel or CRT) may optionally be powered off in POS. This could be accomplished by using the PIIX4E's SUSA# or SUS_STAT2# signals to assert the video controller's STANDBY signal.
Devices may include mass storage, audio, or other devices that will not generate system resume events.

Power Plane Control Using SUS[C:A]# Signals

Power Plane	Suspend Mode (Suspend Mode Signals Asserted by the PIIX4E)			
	Full On (none)	POS (SUSA#, SUS-STAT[2:1]#)	STR (SUS[B:A]# SUS_STAT[2;1]#)	STD (SUS[C:A]# SUS_STAT[2:1]#)
Clock Synthesizer	on	off	off	off
Video Display	on	on / off [1]	off	off
CPU	on	on	off	off
PIIX4E Core	on	on	off	off
Other Devices [2]	on	on	off	off
82443TX	on	on	on	off
DRAM	on	on	on	off
Graphics Controller	on	on	on	off
PIIX4E	on	on	on	on
PIIX4E RTC	on	on	on	on

Notes:
The video display (flat panel or CRT) may optionally be powered off in POS. This could be accomplished by using the PIIX4E's SUSA# or SUS_STAT2# signals to assert the video controller's STANDBY signal.
Devices may include mass storage, audio, or other devices that will not generate system resume events.

7.14 PCI Devices and Definitions

The following definitions for the peripherals corresponds with the BIOS:

Device:	IDSEL	PIRQ	REQ#	GNT#	Comment:
PIIX	AD18				
SLOT 1	AD20	A,B,C,D	0	0	
SLOT 2	AD21	B,C,D,A	1	1	
SLOT 3	AD22	C,D,A,B	2	2	
SLOT 4	AD23	D,A,B,C	3	3	
VGA Controller	AD31				

8 PHOENIX – BIOS

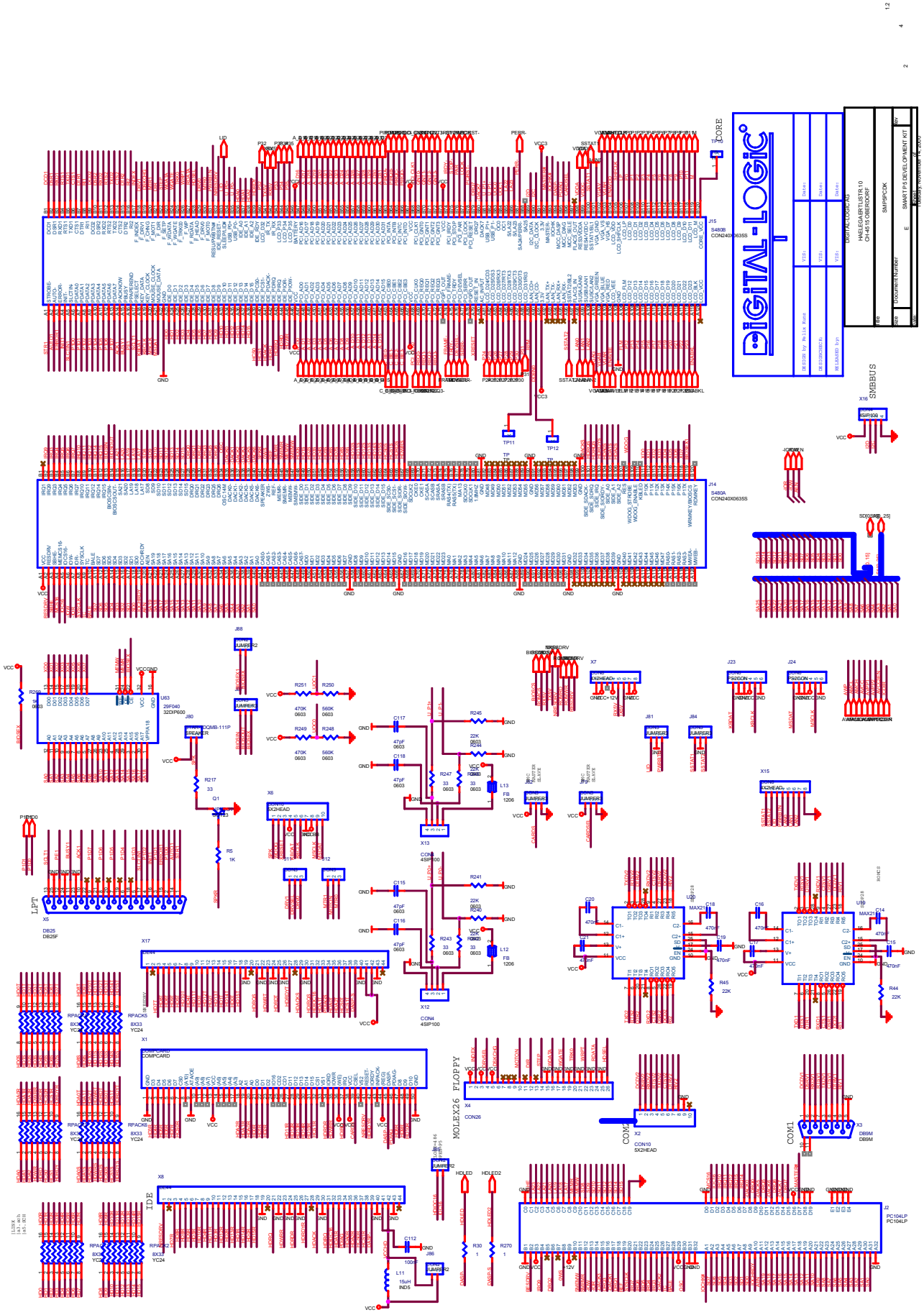
More details are available in the separate BIOS manual on our CD and homepage !

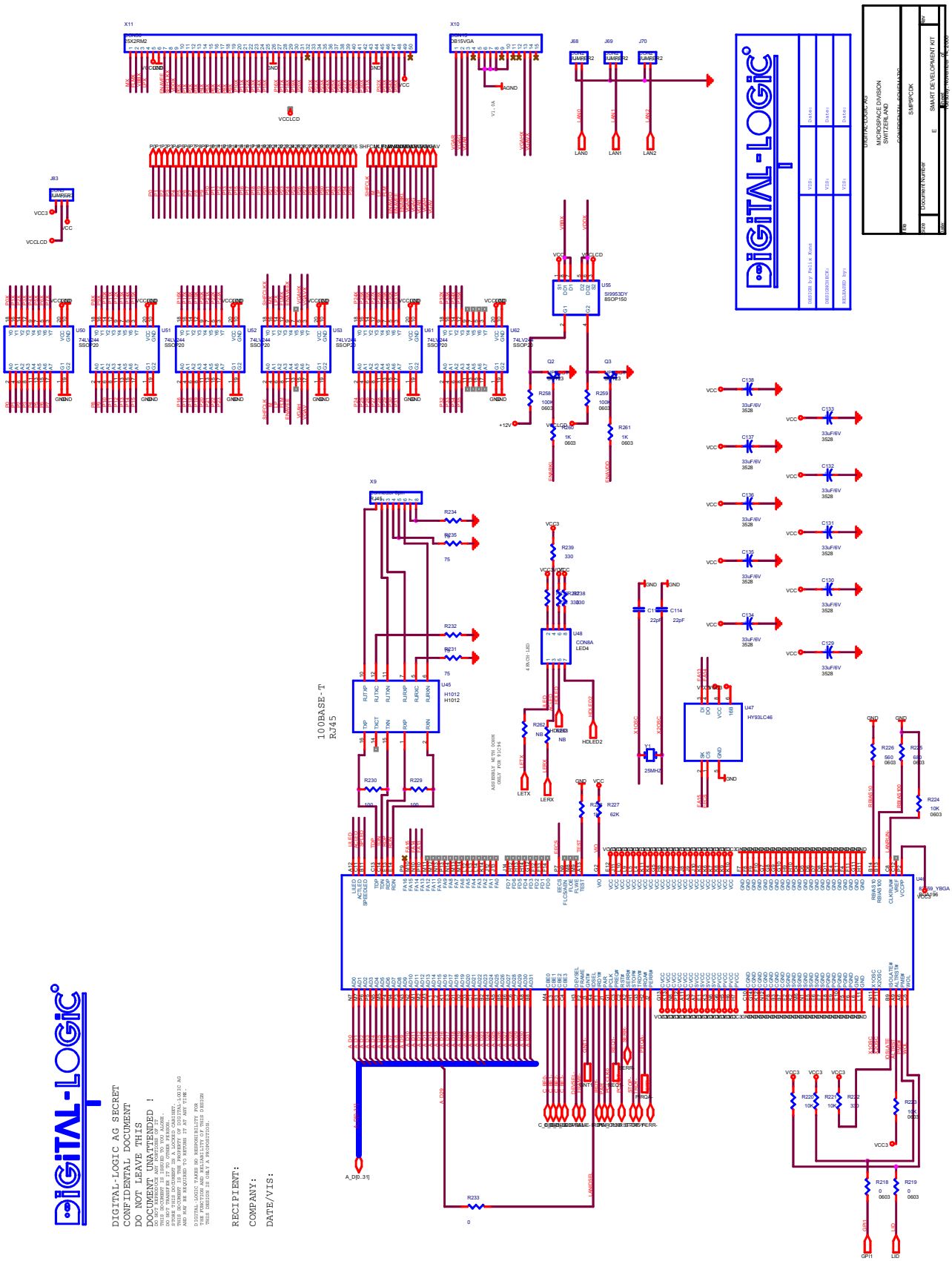
9 SAMPLES SCHEMATICS SM586PC- DK

On the following pages, one will see the schematic for the SM586PC development kit.
This version has been designed for the smartModule until V2.0.
This includes the LAN, ZV- PORT and VIDEO IN devices.

Since V2.1, those devices are not located on the smartModule anymore. Therefore, it is not possible to use the ZV port and VideoIn.

New is a second IDE- PORT inluded, instead of the ZV- PORT.

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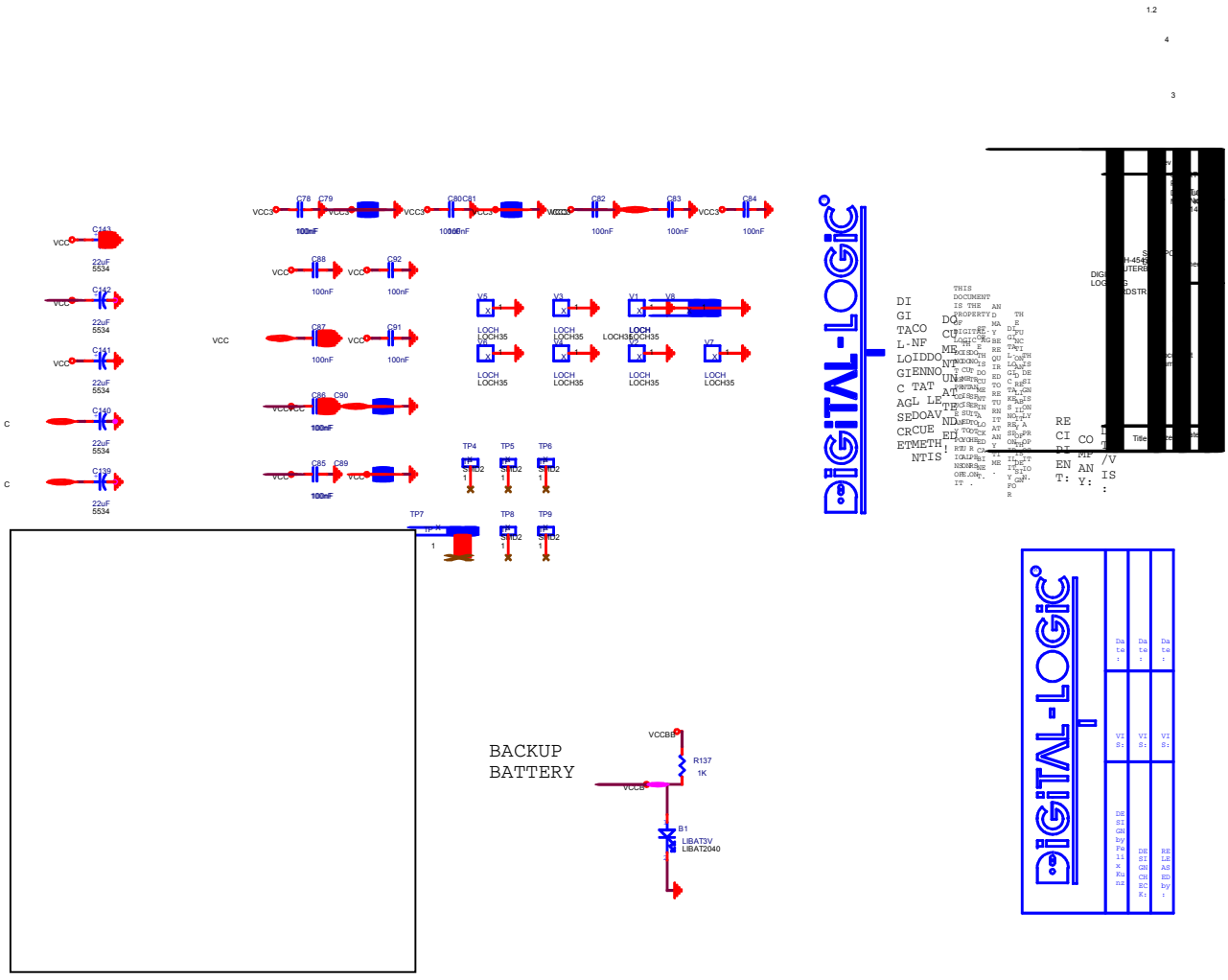
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1K
B1
LIBAT3V
LIBAT2040
SUSC
SUSB
SUSA
SSTAT2
SSTAT1
LAN2
LAN1
LAN0

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