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Specification of the L0DU→ODIN link

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The L0 trigger link [1] between the L0 Decision Unit and the Readout Supervisor 'ODIN' transmits the L0 trigger decisions at a rate of 40 MHz. Each decision should consist of a 16-bit data word:

- Bunch crossing number L0_BID (12 bit)
- L0 trigger decision L0_DECIS (1 bit)
- L0 force bit L0_FORCE (1 bit)
- L0 timing trigger L0_TIM_TRG (1 bit)
- Reserve (1 bit)

15	14	13	12	11 .. 0
Reserve	L0_TIM_TRG	L0_FORCE	L0_DECIS	L0_BID

The bunch crossing number (BID) allows the Readout Supervisor to check the synchronization of the L0DU. It should be provided by a local counter in the L0DU with a modulus of 3563 and must be aligned by applying an offset at each Bunch Counter Reset (BCR) such that it marks the current trigger being processed locally. Since the BCR is applied at the end of the L0 pipeline in the L0 FE electronics, the offset is used to compensate for the transmission time from the L0DU to the L0 FE electronics. As shown in figure 3 the offset is the sum of the time spent to process the bunch identifier in the L0DU, the transmission time to the Readout Supervisor, the processing time in the Readout Supervisor, and the transmission time to the FE electronics, that is $\sim \delta_{\text{L0DU internal}} + \delta_{\text{L0DU-ODIN}} + \delta_{\text{ODIN internal}} + \delta_{\text{TTC}}$. The BID from the L0DU and the local BID in the Readout Supervisor is sampled simultaneously in a register in the Readout Supervisor. Once the BID is correctly set up in the Readout Supervisor, the BID offset in the L0DU can be deduced from the difference between the two values in the Readout Supervisor.

In order to monitor the L0 trigger processing it might be useful to produce special triggers or accept randomly at low rate some trigger conditions that would normally be rejected. The L0 force bit allows the L0DU to request that the Readout Supervisor forces the trigger to be accepted at Level-1. The L0 decision bit should also be set for these triggers.

In order to align the entire L0 path to 160 cycles, the L0 system might need to incorporate additional pipelining. The Readout Supervisor will have a L0 pipeline of adjustable length of up to 16 cycles in addition to a fixed length pipeline of up to 7 cycles to handle L0 timing triggers[1]. The L0 timing trigger is intended for timing alignment runs. The trigger should be generated on an event that allows verifying the timing of all the synchronous electronics, such as an isolated interaction. The L0DU should set the timing trigger bit at the same time with the to the actual trigger decision corresponding to the special event transmitted via the L0_DECIS line. The timing trigger bit is not fed through the fixed L0 pipeline in the Readout Supervisor. Upon receiving the timing trigger the Readout Supervisor can thus generate a series of trigger accepts before and after the special event (up to a maximum of 15 = 7 before + actual timing

[1] The exact value will be decided as soon as the L0 latency budget has been re-estimated carefully.

trigger + 7 after) and make sure that they are kept at Level-1. A priori there is no need to control the rate of the timing triggers. Like with physics triggers, the Readout Supervisor ensures that the rate is maintained at an acceptable level. However, it might still be a useful option to be able to scale the timing triggers.

The timing of the transmission or the timing of the sampling point in the Readout Supervisor might require some adjustments. Several options exist:

- The Readout Supervisor has a programmable function to sample the L0 trigger words on the positive edges of the clock or the negative edges, and in the latter resynchronizes in the next clock cycle to positive clock edges.
- Length of L0DU-ODIN link
- Fine adjustment of the clock phase in the TTCrx of the L0DU.

The last might also affect the sampling at the trigger input links to the L0DU.

The trigger word should be transmitted over a point-to-point parallel 16-bit LVDS link using a twisted pair ribbon cable with 17-pairs. The LVDS pairs are terminated in the standard manner with a 100ohm resistor at the receiver. The link has been implemented and tested over a distance of 10m using the following components:

- Receiver chips: Maxim 9179 EUE (Quad LVDS receiver with hysteresis)
- PCB connector: 3M Pak 100 4-wall header with latch, 34 pin (3M 3431-5502 or 5602)
- Cable connector: 3M Pak 100 Wiremount socket, 34 pin (3M 3414-6600 or 6634)
- Ribbon cable: Twisted pair flat 34C 1.27mm AWG28 (SCEM 04.21.22.434.8)

Figure 1 below shows the pin configuration of the connector and figure 2 shows the actual layout of the connector with the position of pin 1. Notice the order of the LVDS+/- and that the 17^{th} pair (pins 33 and 34) should be ground.

Several options have been foreseen for the grounding scheme between the L0DU and the Readout Supervisors. The best solution will have to be investigated during the installation in the pit.

- The TFC racks and the L0DU rack will be on the same power ground. An additional ground cable between the TFC racks and the L0DU rack has been foreseen to improve the ground connection.
- One pair of grounds in the L0DU-ODIN link. If it is found that it is better to avoid connecting the grounds to avoid loops, it should be done at the level of the cable.

The pair called L0_STROBE is not used but is instead a spare data connection.

The TFC test board ‘FREJA’ has been used as L0DU for extensive testing of the L0 trigger path. The transmitter side has been implemented using the National DS92LV090A (9 channel bus LVDS transceiver).

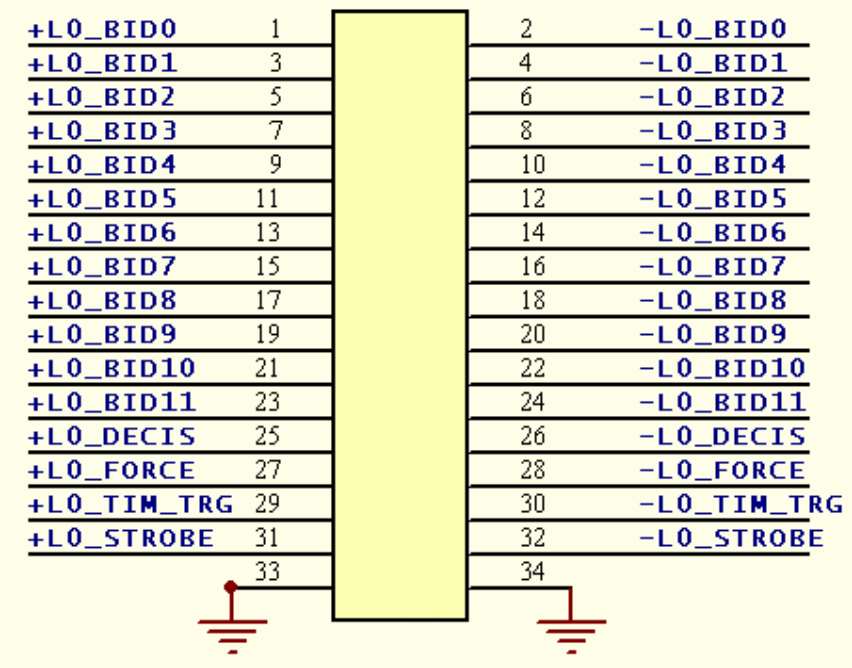

Figure 1 : L0 trigger input on the Readout Supervisor. The pair called L0_STROBE is not used anymore but is instead a spare connection.

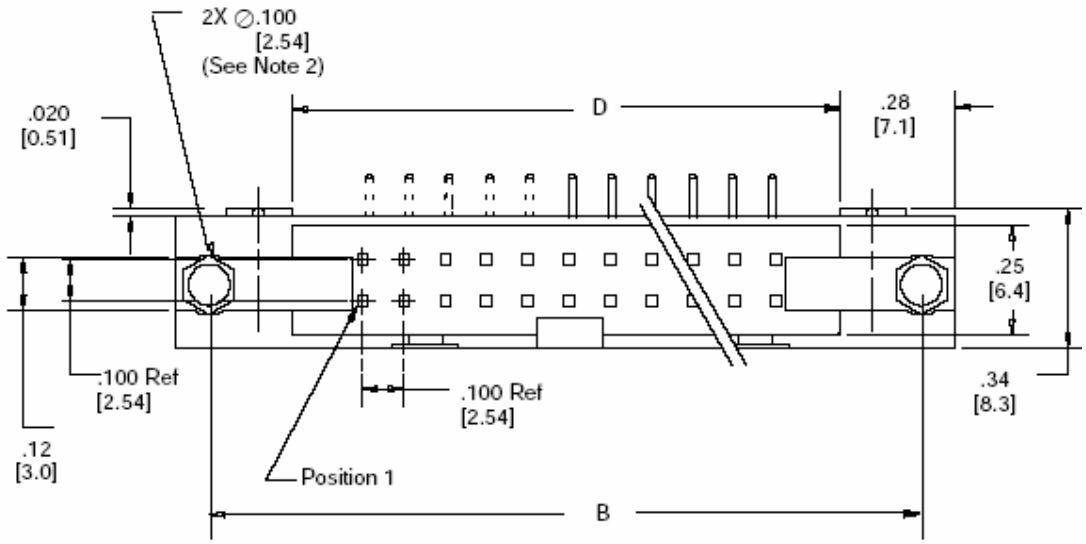

Figure 2: Connector layout with the position of pin 1 for the connector 3M 3431-5502.

[1] Readout Supervisor Design Specifications, R. Jacobsson, B. Jost, Z. Guzik, LHCb 2001-012 DAQ.

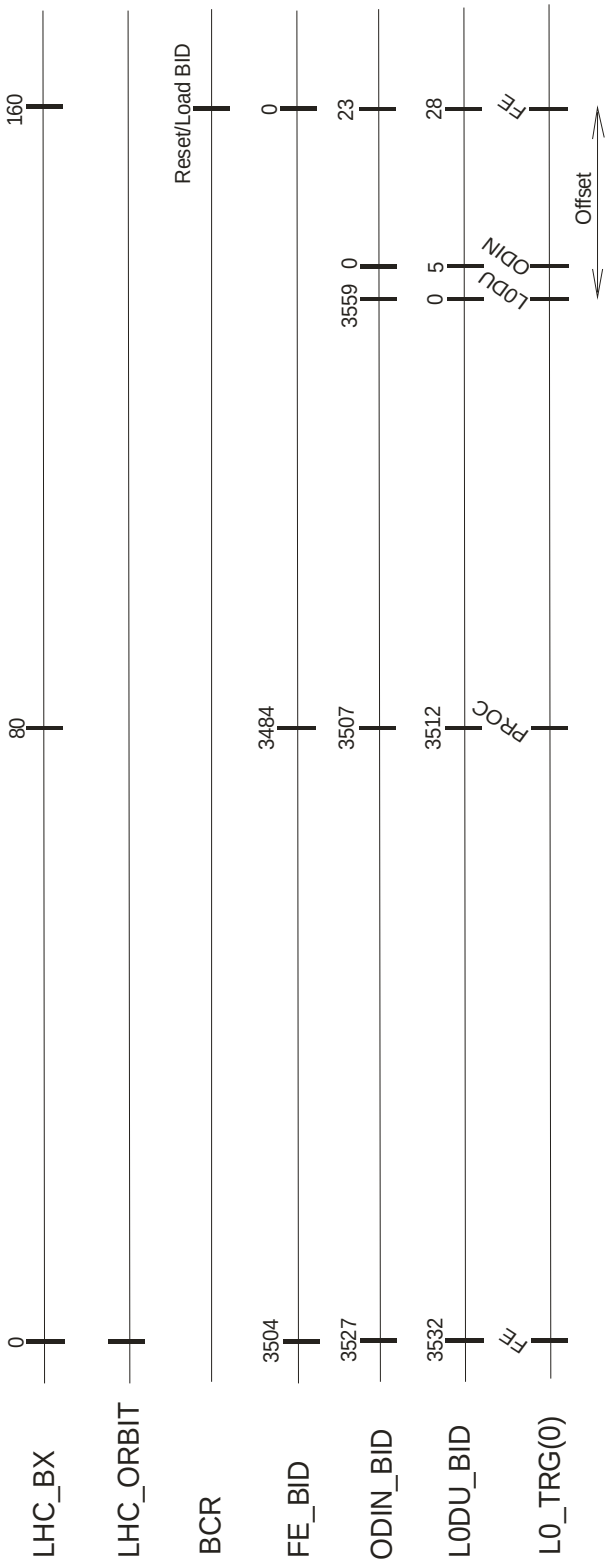

Figure 3: Example of a timing alignement along the L0 trigger path. The LHC_BX is the actual LHC bunch crossing number and the LHC_ORBIT is the orbit signal marking the turns of the beams as it occurs at the LHCb interaction point. The Bunch Counter Reset (BCR) is sent such that it resets the Bunch crossing identifier in the front end (FE_BID) at the end of the 160 deep L0 pipeline. ODIN_BID and L0DU_BID shows the current value of the local bunch crossing identifier counters in the Readout Supervisor and in the L0DU. L0_TRG(0) shows the propagation of the L0 trigger for crossing 0 along the L0 trigger path.